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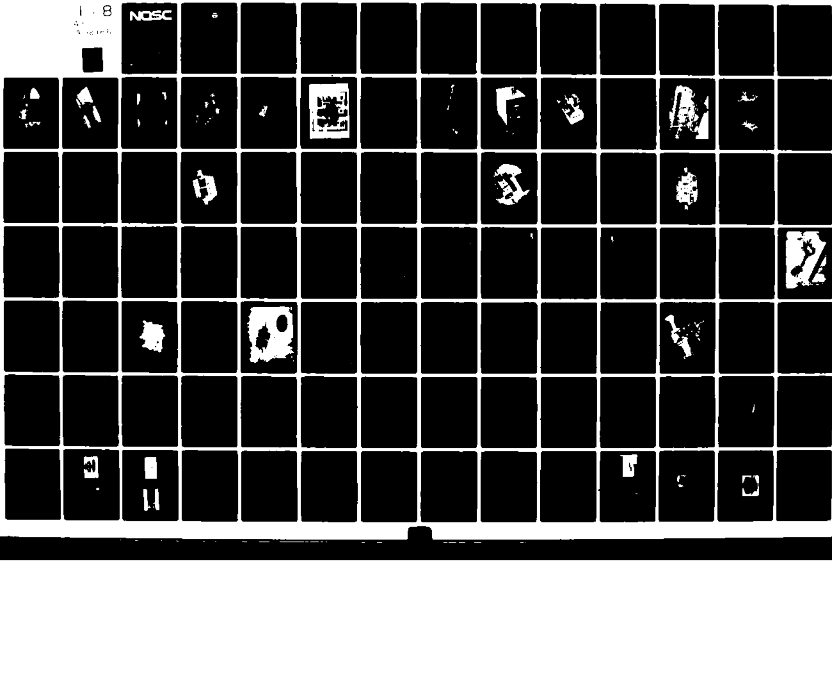

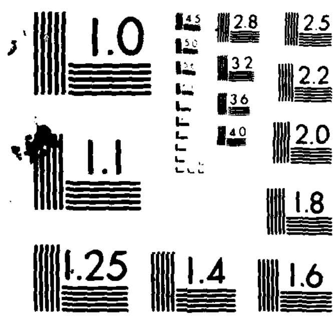

MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS 1963 A

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NOSC TD 457

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EHF SATCOM TECHNOLOGY WORKSHOP 4-6 AUGUST 1981

KA Brodeur
KR Casey

September 1981

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NAVAL OCEAN SYSTEMS CENTER
SAN DIEGO, CALIFORNIA 92152

NAVAL OCEAN SYSTEMS CENTER, SAN DIEGO, CA 92152

AN ACTIVITY OF THE NAVAL MATERIAL COMMAND

SL GUILLE, CAPT, USN
Commander

HL BLOOD
Technical Director

ADMINISTRATIVE INFORMATION

Work was performed under program element 62712N subproject XF12143555 (NOSC 814-CM03), by the EHF Communications Systems Program Branch (Code 8143).

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H. J. Wirth, Head
SATCOM & HF Communications
Systems Division

Under authority of
H. D. Smith, Head
Communications Systems
and Technology Department

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MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LINCOLN LABORATORY

K-Band Technology Development For EHF Satellite Application

C. D. BERGLUND, R. J. LENDER, M. L. STEVENS

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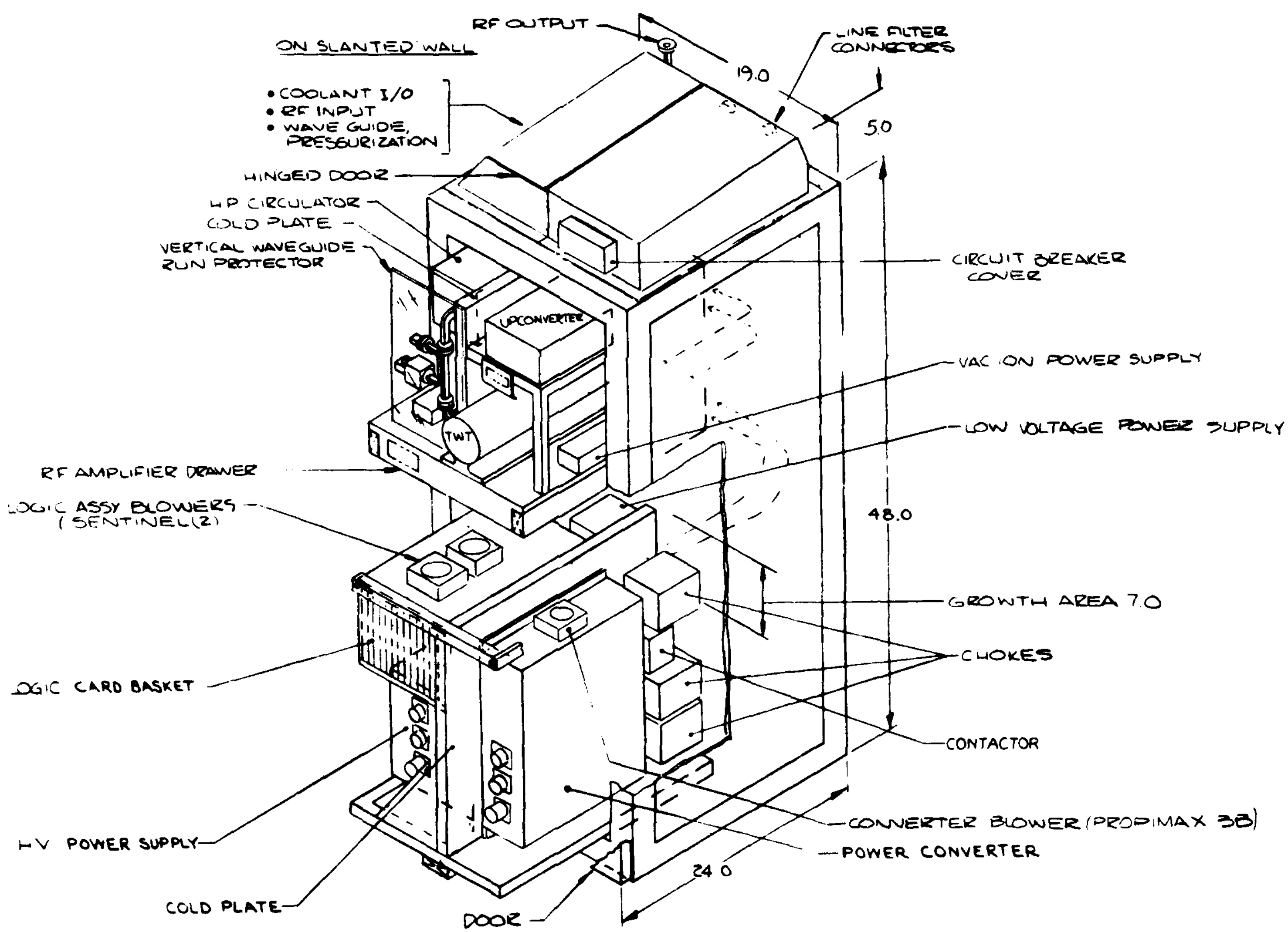
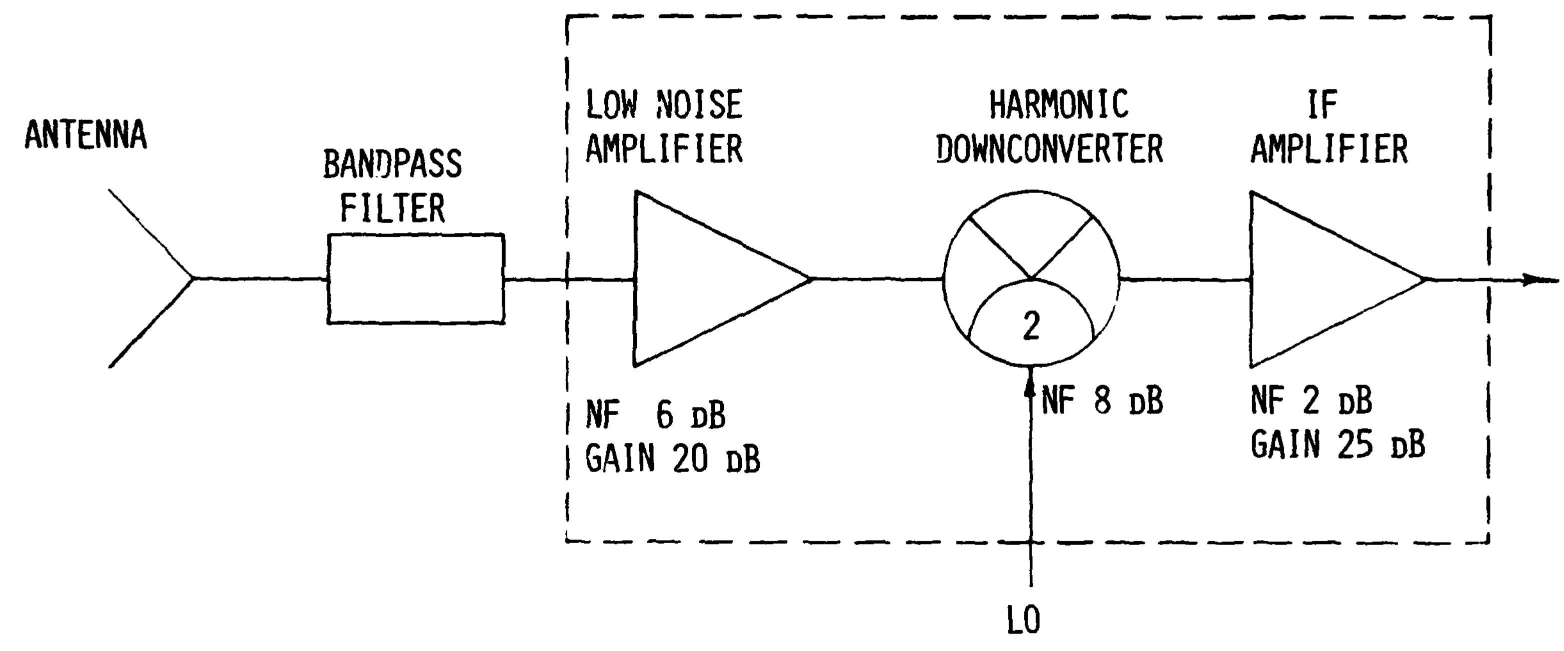
20 - 21 GHz RECEIVER FRONT END DESIGNS
- SPECIFICATIONS
- DEVICE CHARACTERIZATION
- AMPLIFIER PERFORMANCE

20 - 21 GHz GALLIUM ARSENIDE MESFET AMPLIFIER DEVELOPMENT
- DEVICE DEVELOPMENT
- DEVICE CHARACTERIZATION
  - LOAD PULL TECHNIQUE/TUNEABLE SLABLINE CIRCUIT
  - LARGE SIGNAL "S-PARAMETER"/FIXED MICROSTRIP CIRCUITS
- DEVICE PERFORMANCE
- AMPLIFIER DESIGN AND PERFORMANCE

CONCLUSION

Q-BAND HPA CABINET

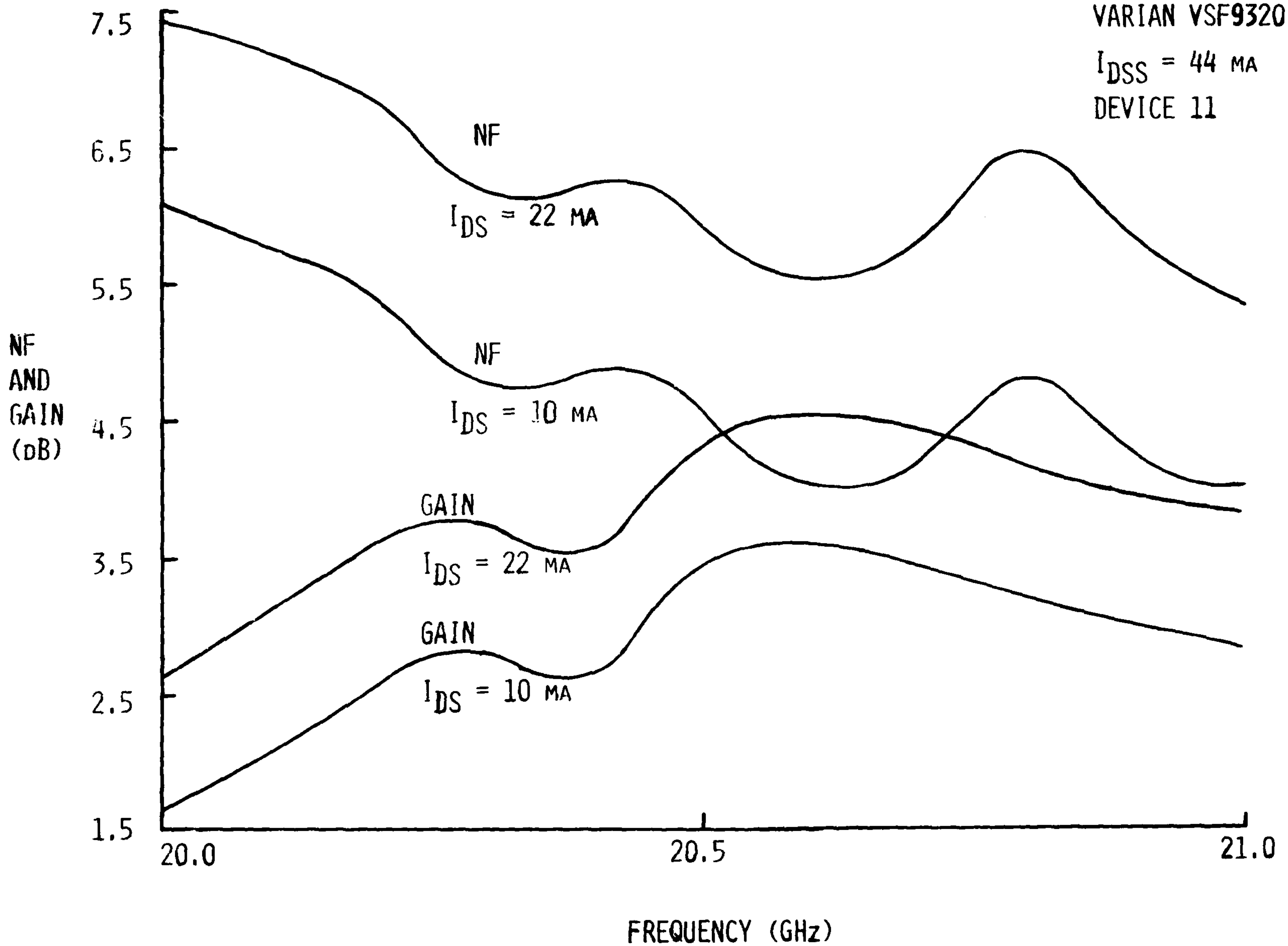




- NOISE FIGURE ≤ 6.5 dB
- SMALL SIZE, VOLUME = 6 IN^3
- LOW COST

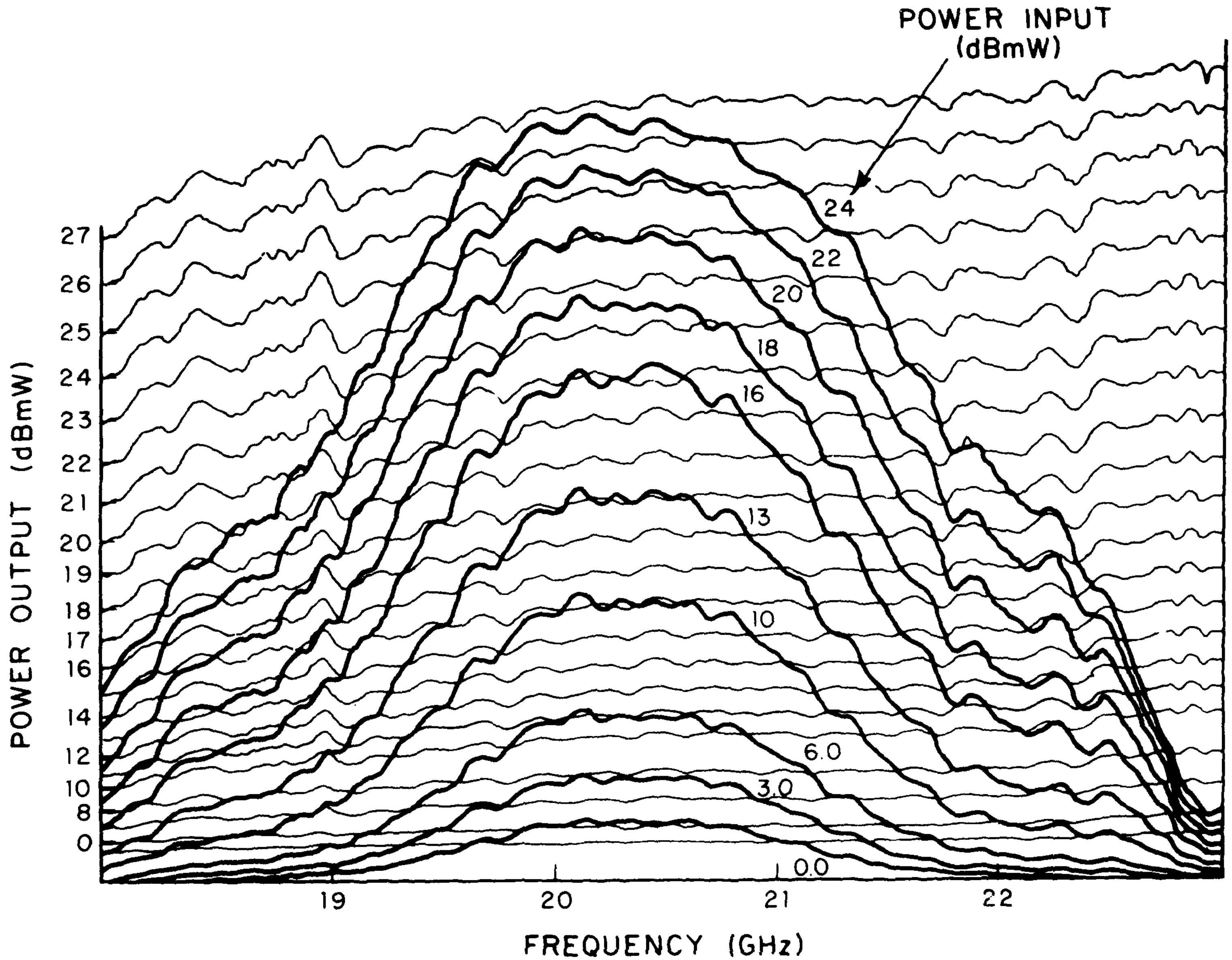
Block Diagram – 20 –21 GHz Receiver Front-End

Performance of Low Noise Amplifier vs Bias

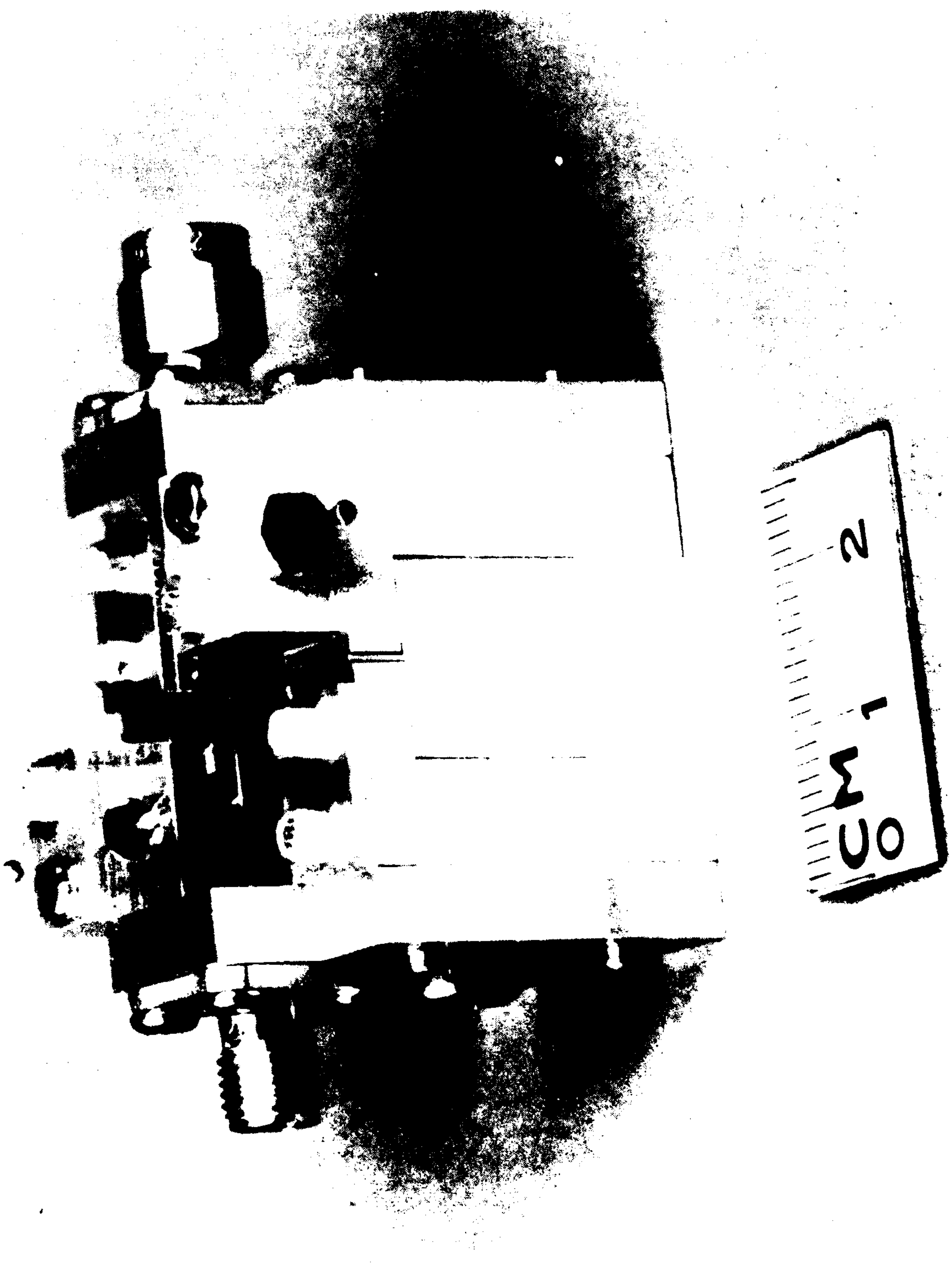


K-Band FET Development Specification

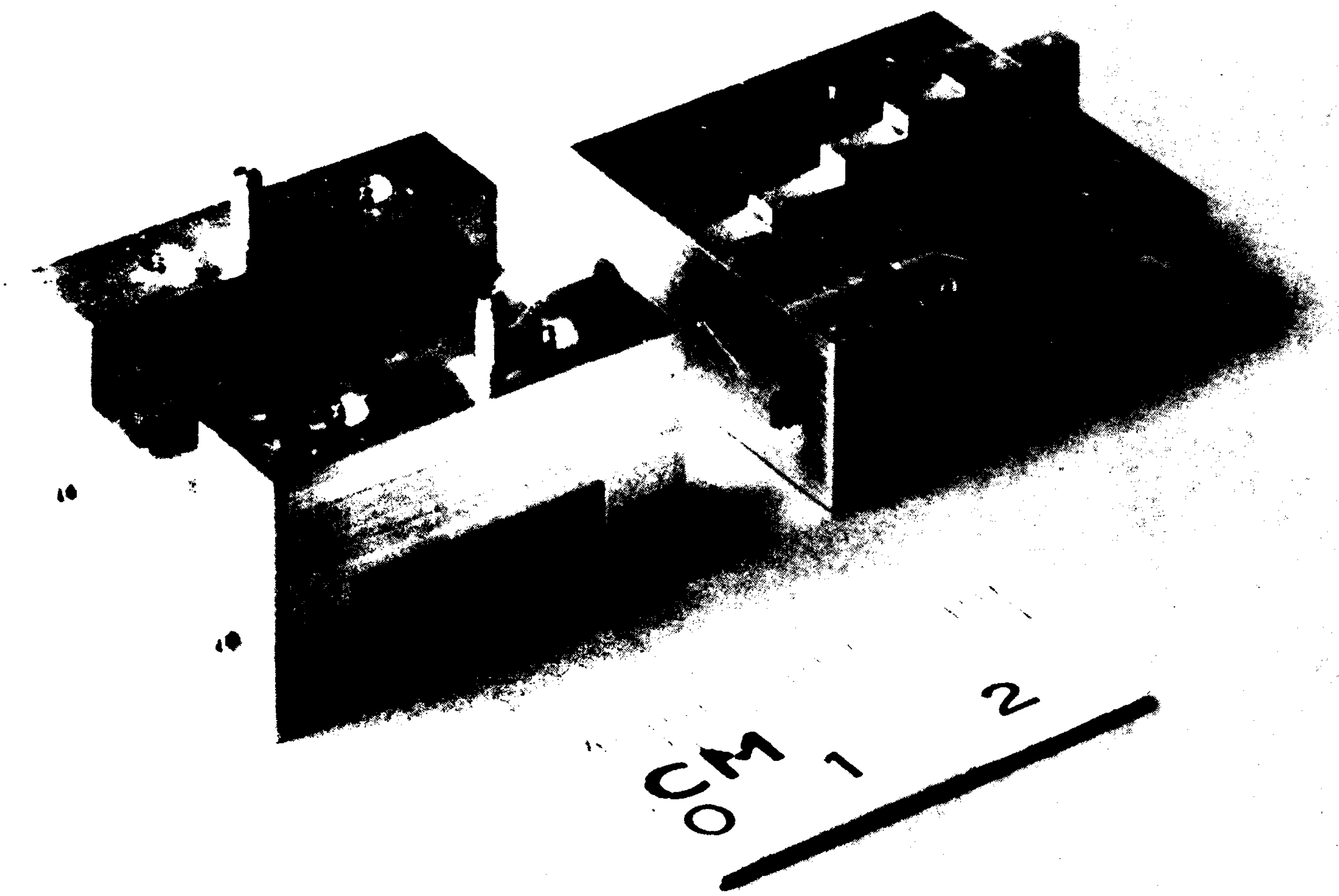
	I		II		III	
PERFORMANCE AT 21 GHz	GOAL	MINIMUM	GOAL	MINIMUM	GOAL	MINIMUM
POWER OUTPUT	1.0 W.	0.5 W.	--	1.0 W.	--	0.1 W.
POWER ADDED EFFICIENCY	20%	15%	20%	15%	20%	--
GAIN	5.0 dB	4.0 dB	5.0 dB	4.0 dB	10 dB	8 dB
CHANNEL TEMPERATURE RISE	< 100°C		< 100°C		< 100°C	
DELIVERABLES	50		60		100	
CONTRACTOR	MSC		MSC		MSC DEXCEL HUGHES	
STATUS	COMPLETED AUGUST 1980		SCHEDULED COMPLETION OCTOBER 1981			



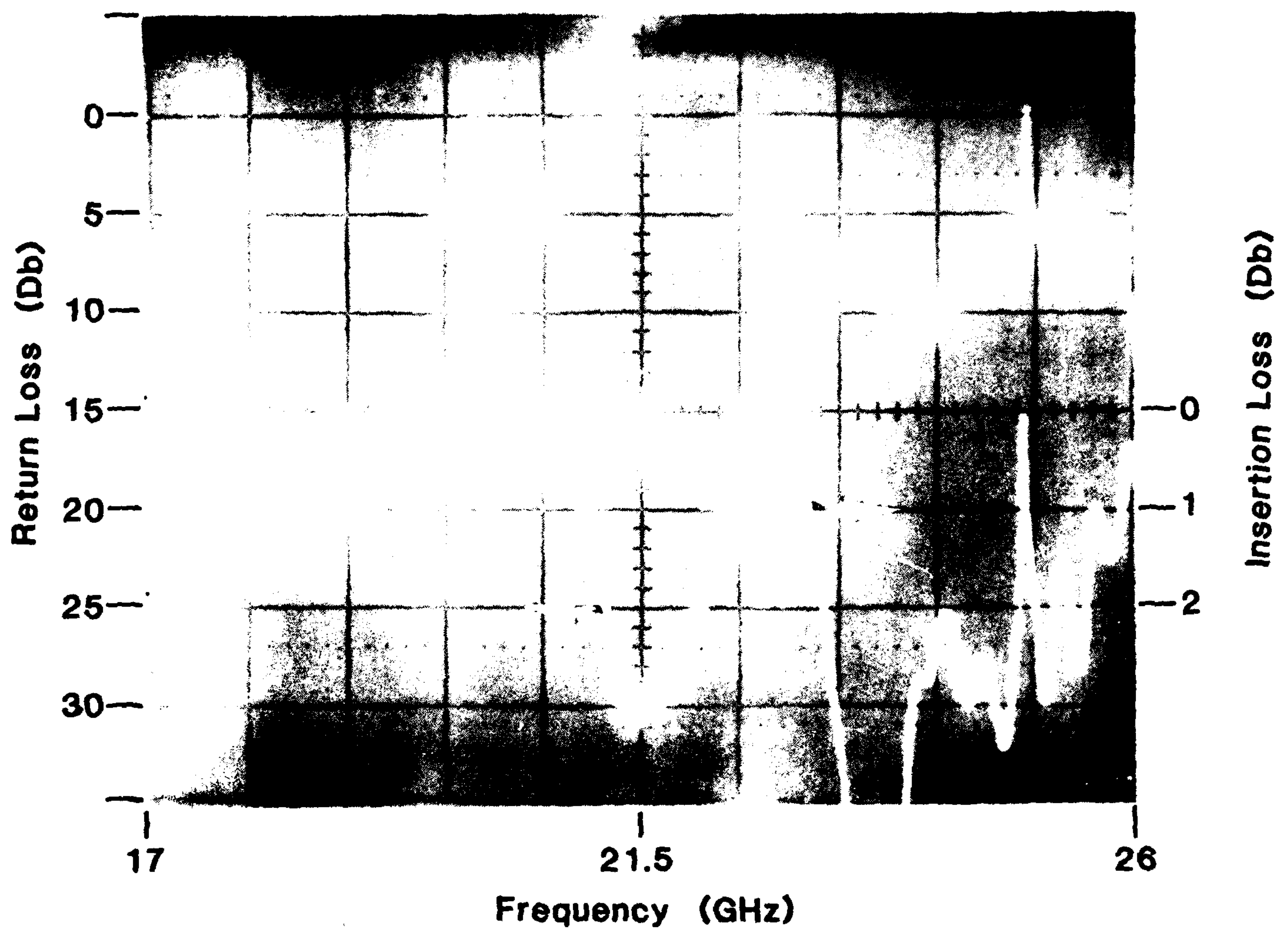
Microstrip Amplifier Power-Bandwidth Response.



Low Frequency FET Test Fixture

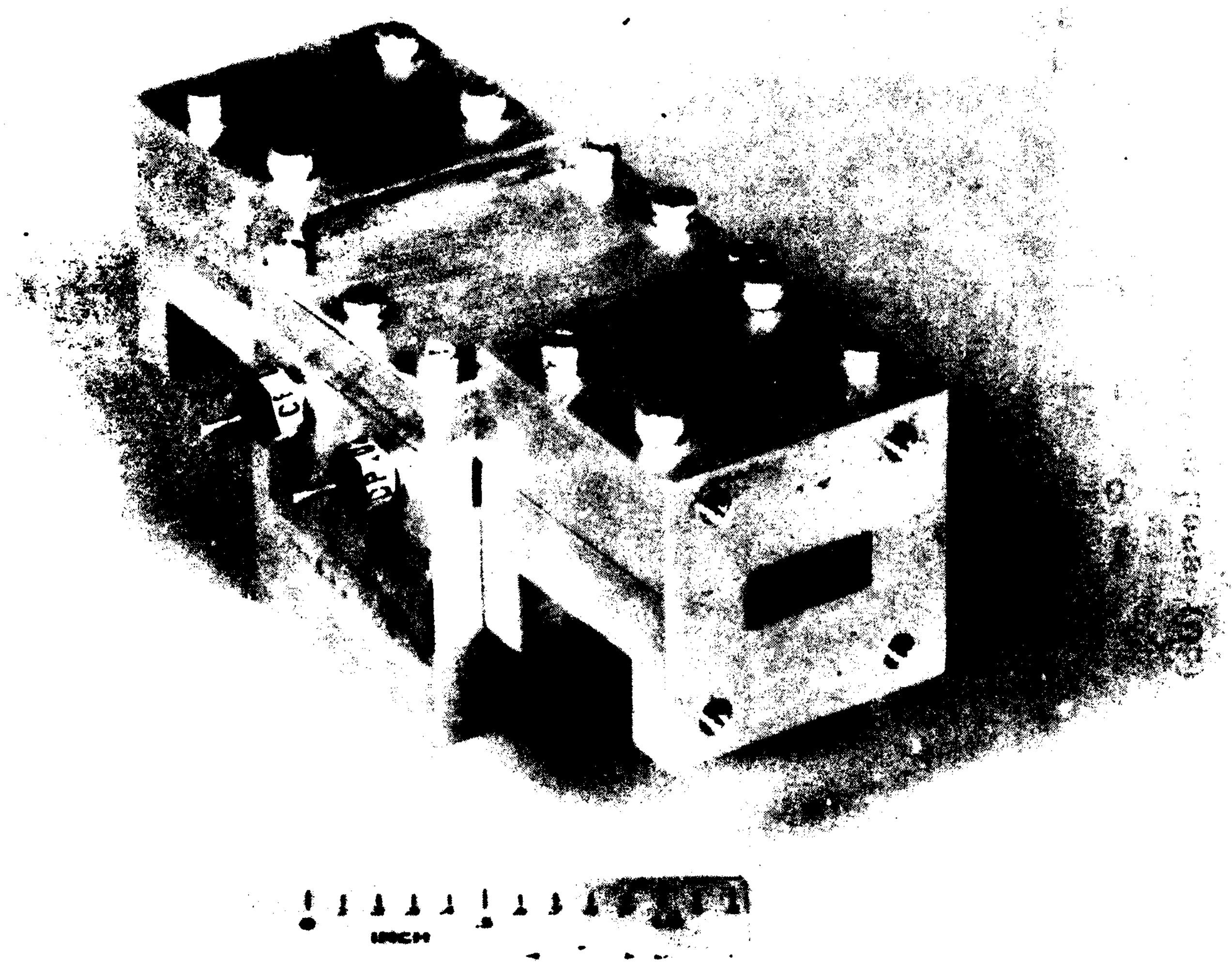


Ridge-Transformer Waveguide to Microstrip Transition

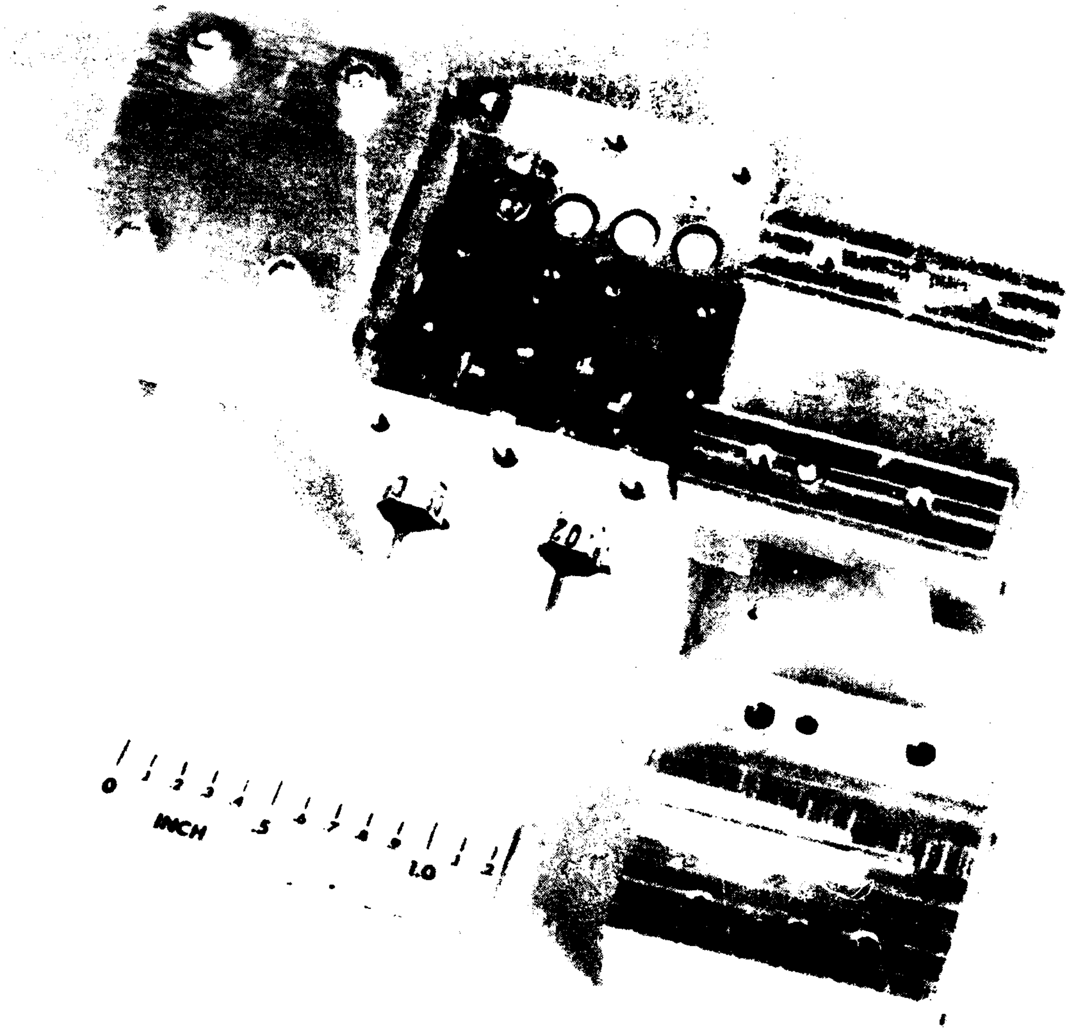


Ridge-Transformer Performance

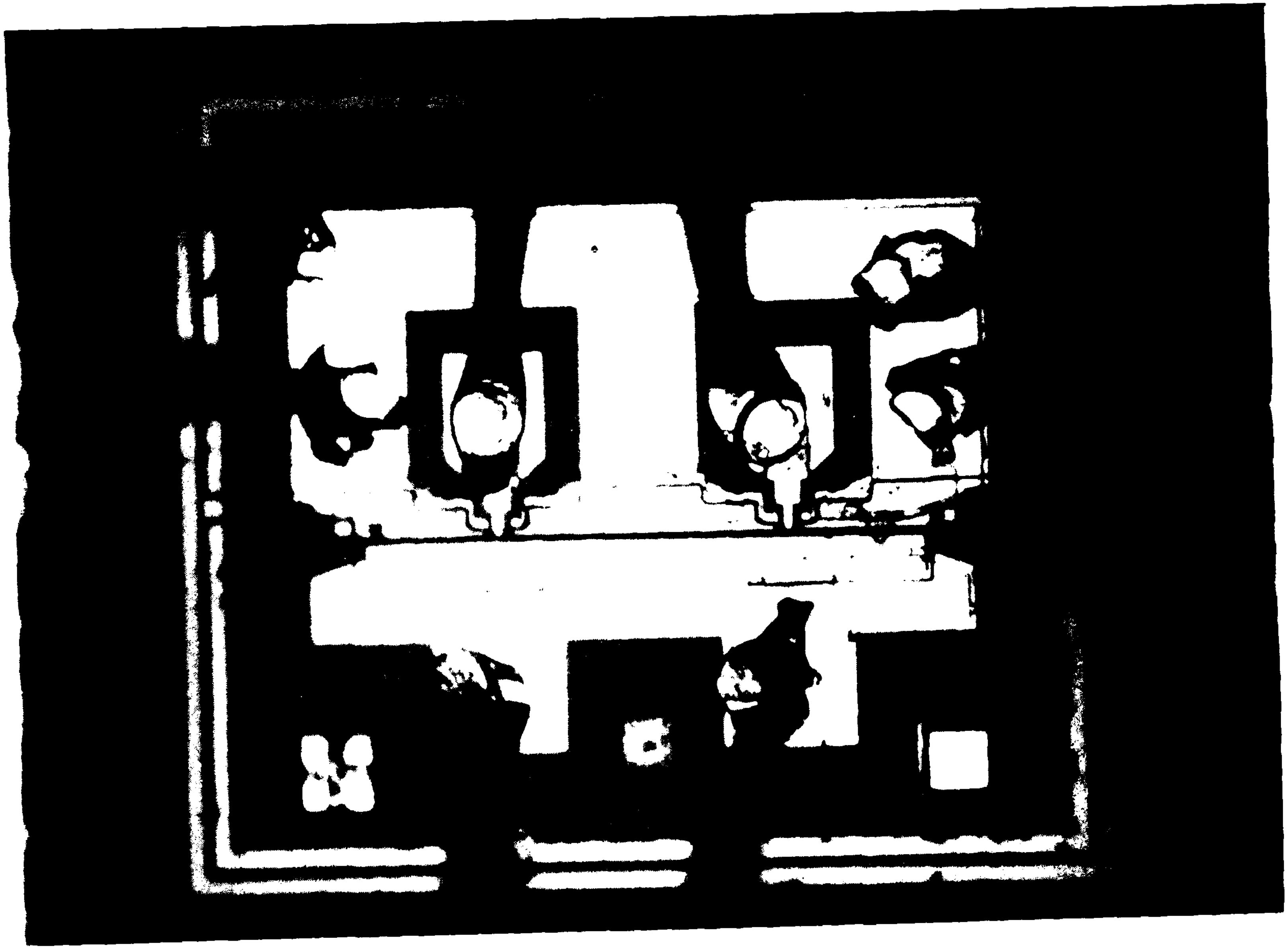
C63-3123



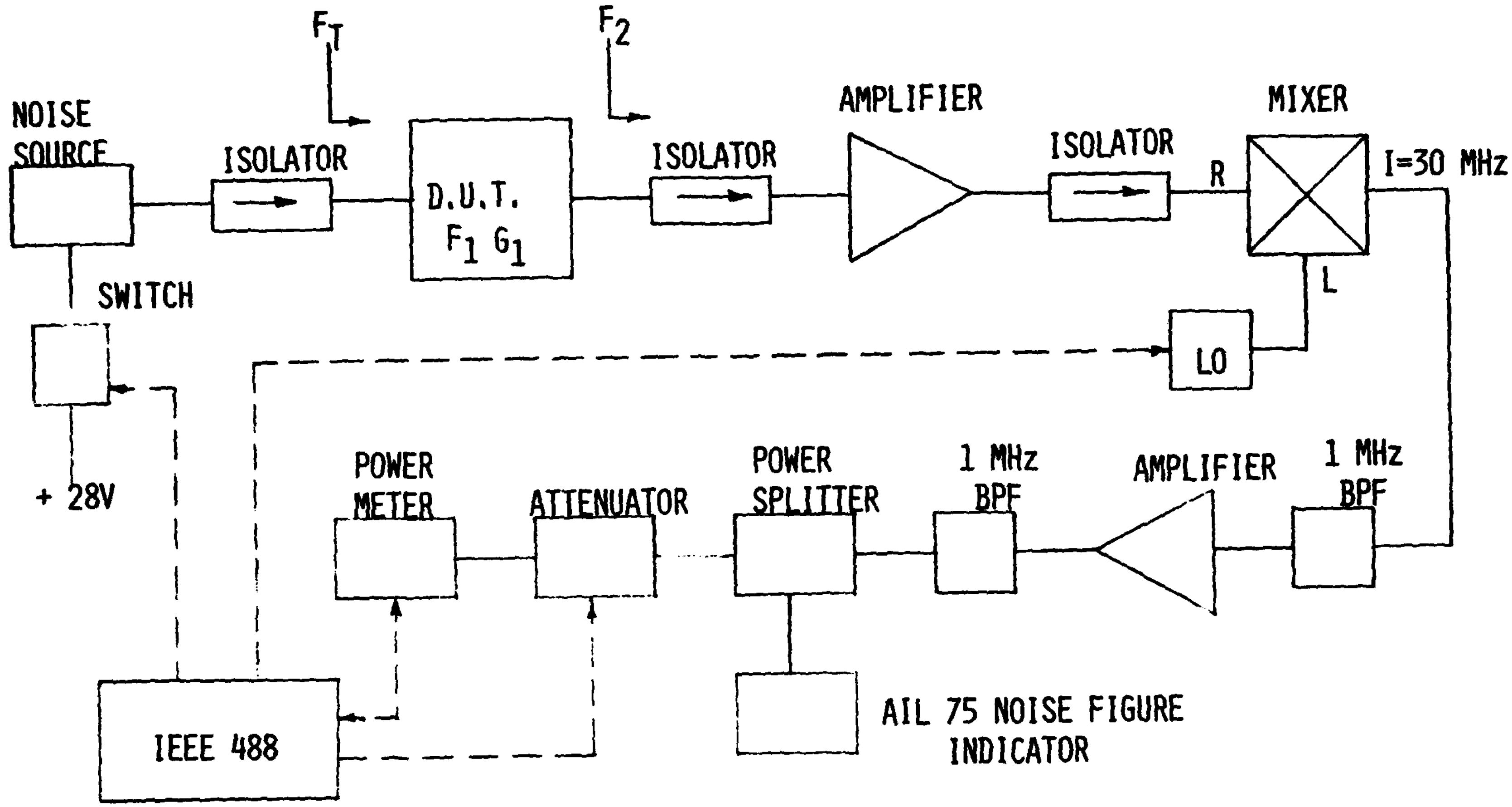
K-Band Low Noise Amplifier (with cover)



K-Band Low Noise Amplifier (without cover)

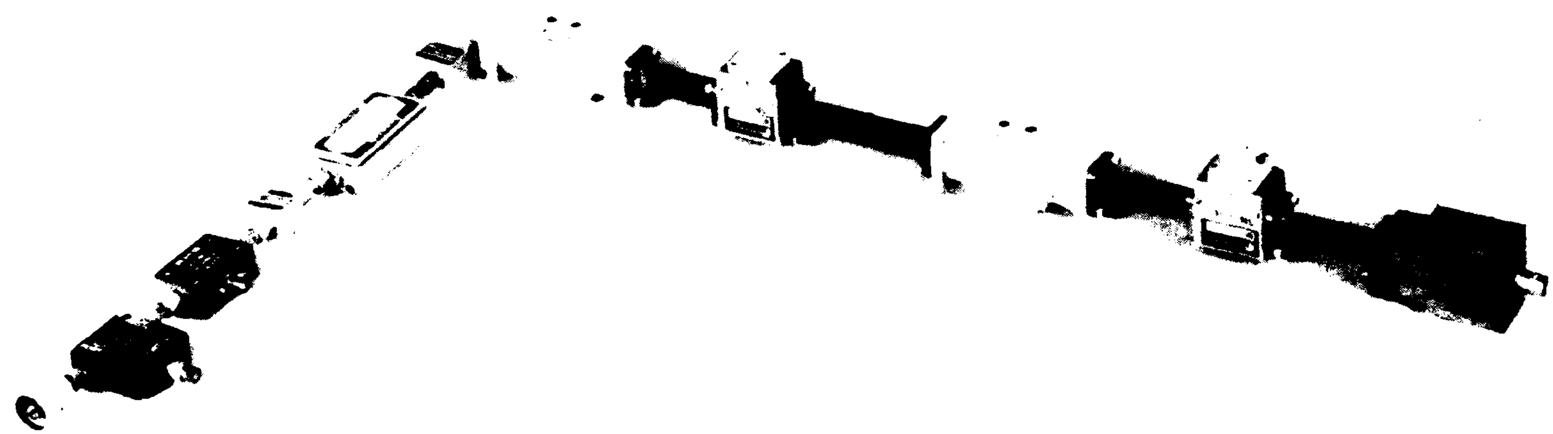


NEC 13700 Transistor



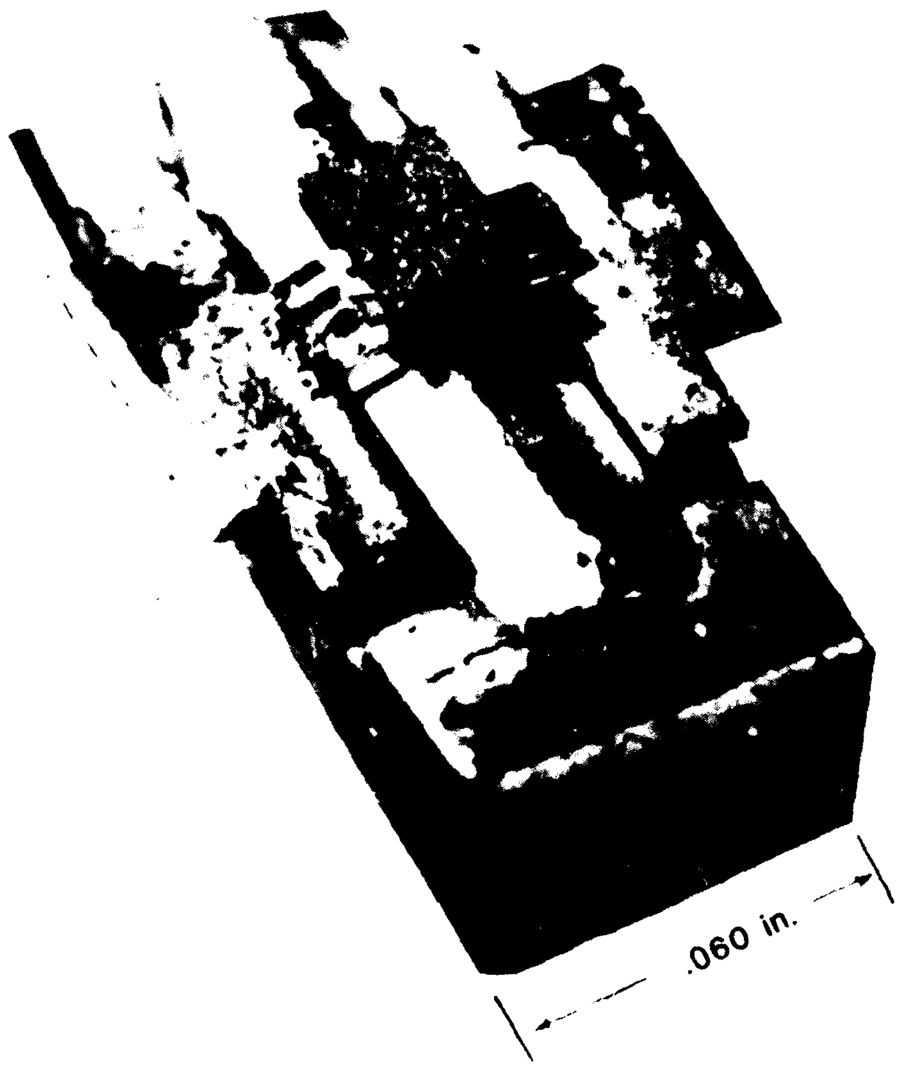
$$F_T = F_1 + \frac{F_2 - 1}{G_1}$$

Block Diagram – Automatic Noise Figure Measurement System

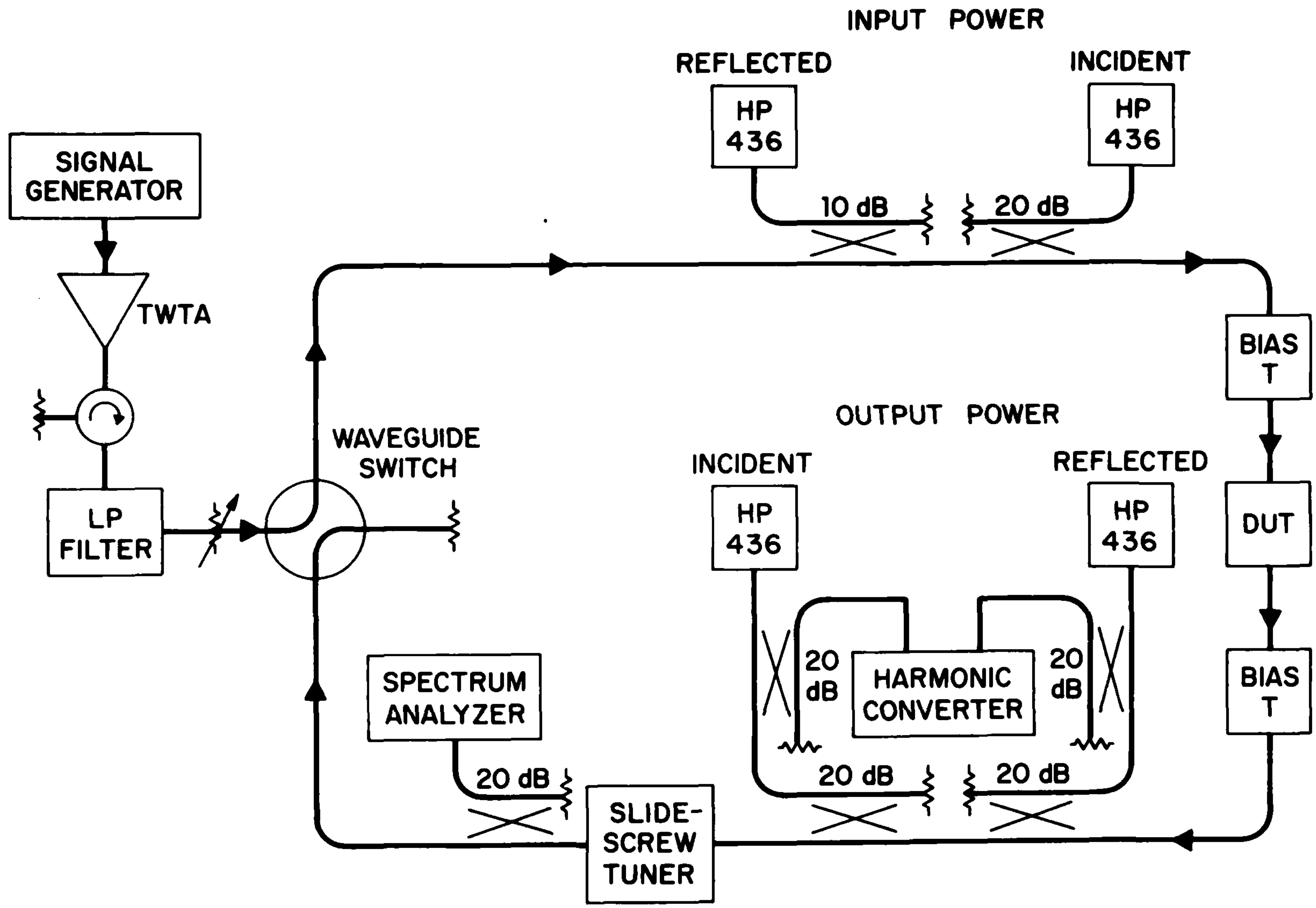


Noise Figure Measurement Instrumentation

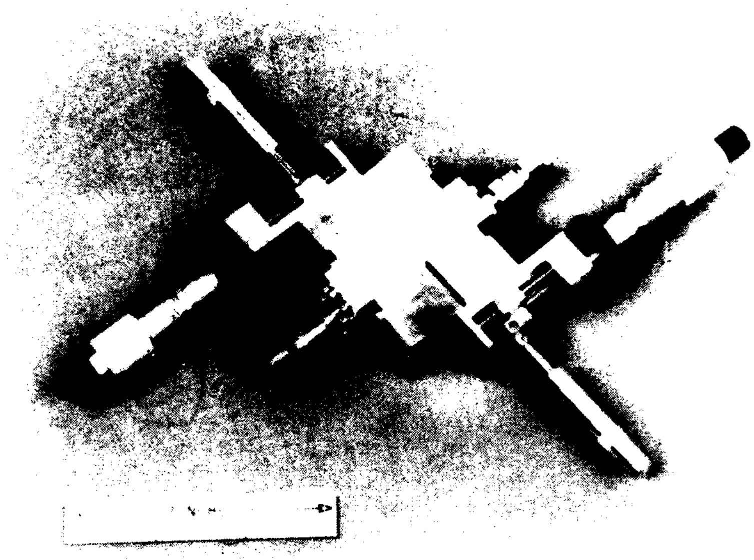
Hot/Cold Waveguide Load



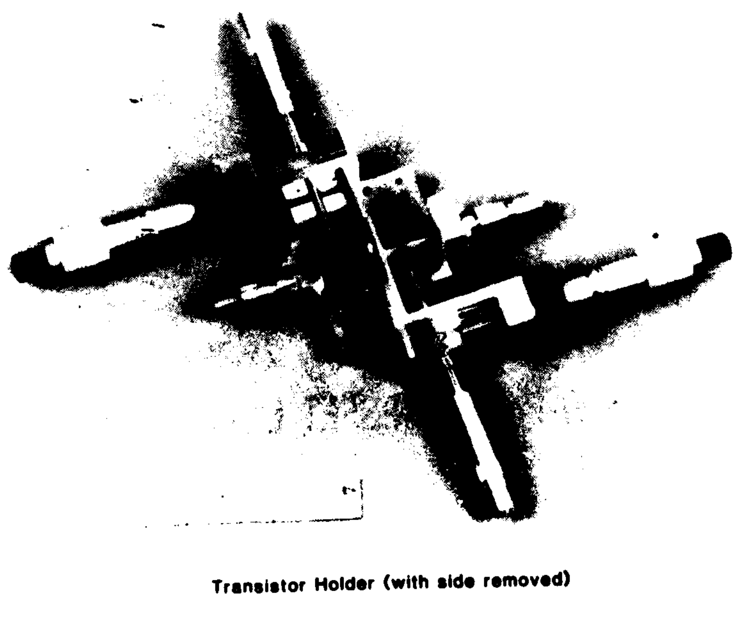
K-Band 0.5W. GaAs MESFET



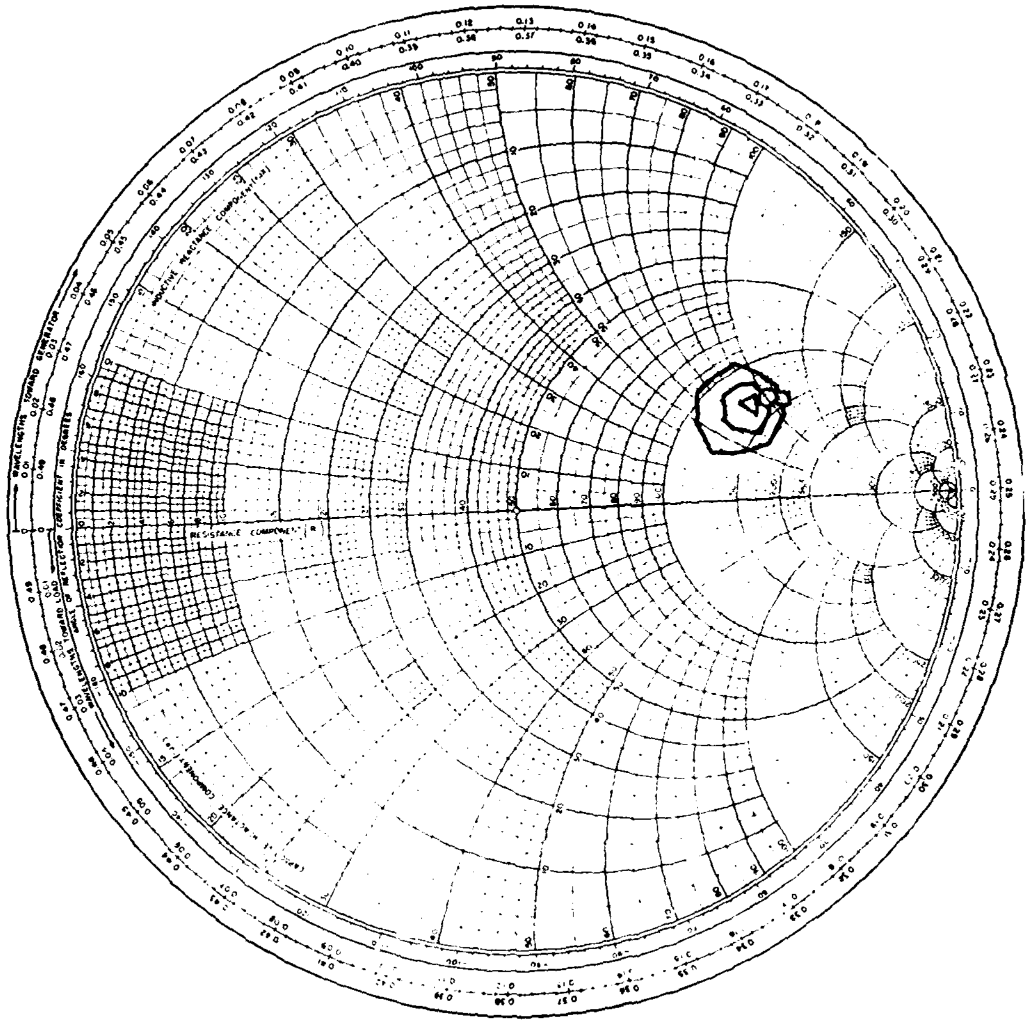
Block Diagram of Load-Pull Measurement Set-Up.



Slabline Transistor Holder

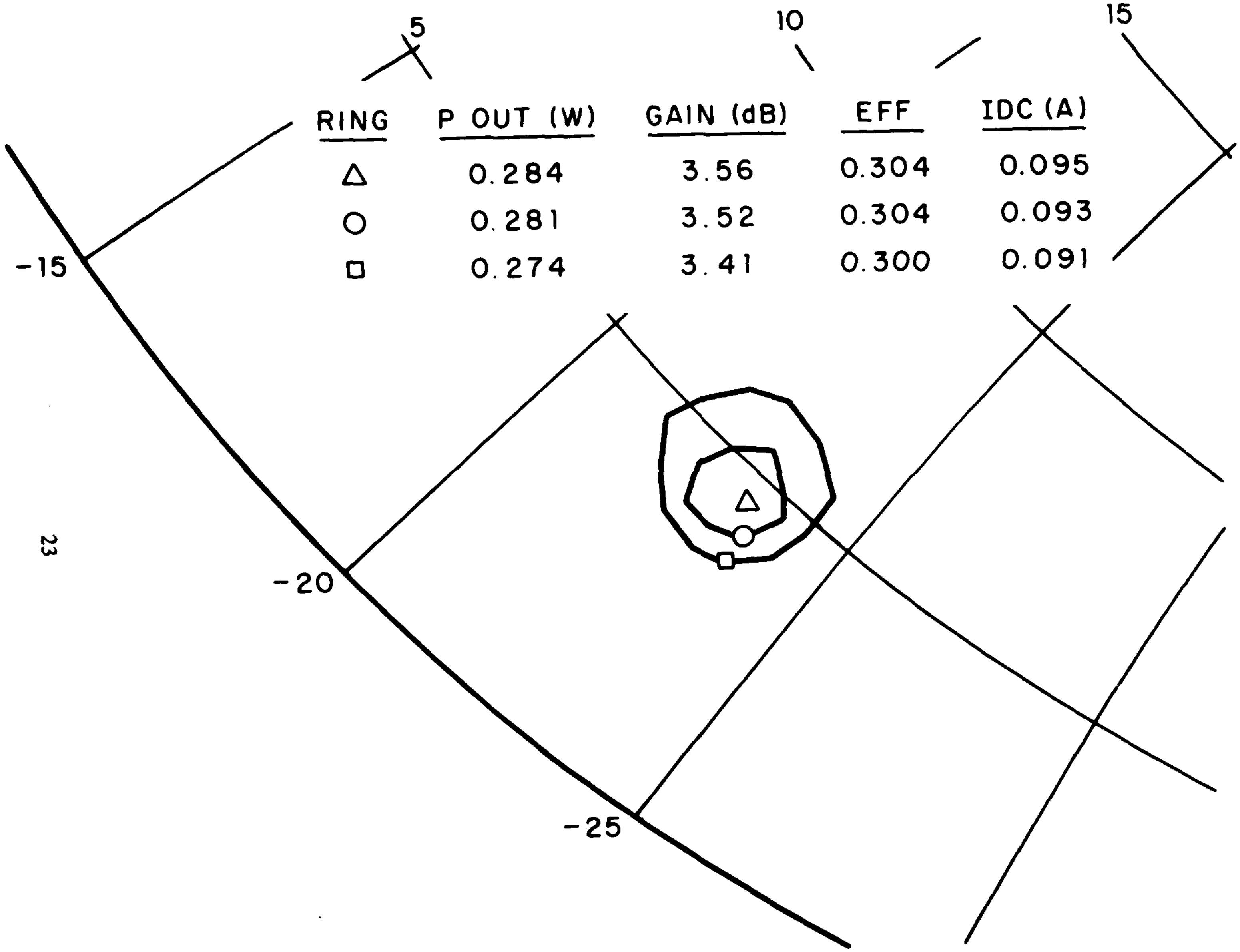


Transistor Holder (with side removed)



RING	P OUT (W)	GAIN (dB)	EFF	IDC (A)
△	0.284	3.56	0.304	0.095
○	0.281	3.52	0.304	0.093
□	0.274	3.41	0.300	0.091

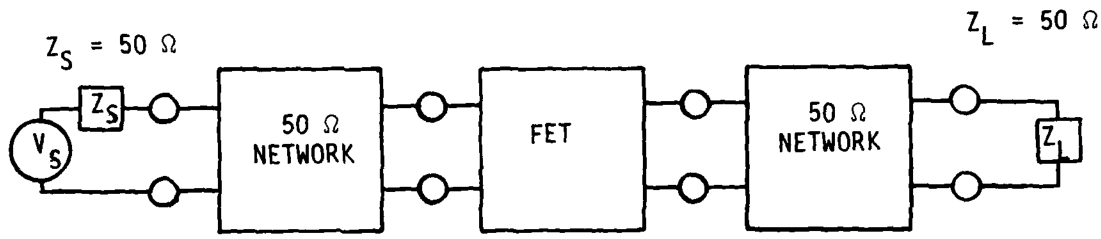
0.5 W Power MESFET Load-Pull Measurement.



RING	P OUT (W)	GAIN (dB)	EFF	IDC (A)
△	0.284	3.56	0.304	0.095
○	0.281	3.52	0.304	0.093
□	0.274	3.41	0.300	0.091

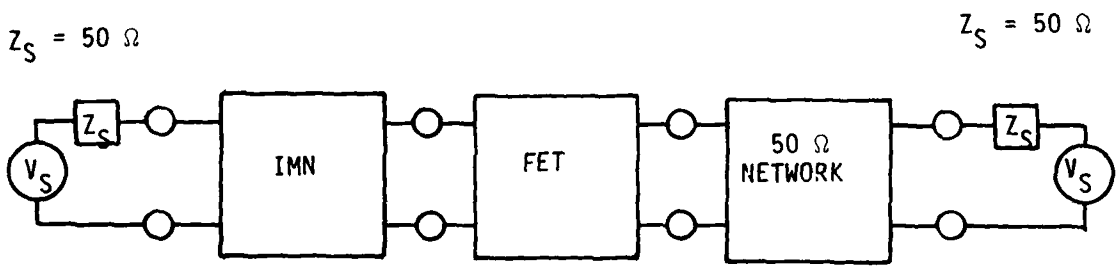
De-Embedded Load-Pull Data.

Large Signal FET Characterization Procedure



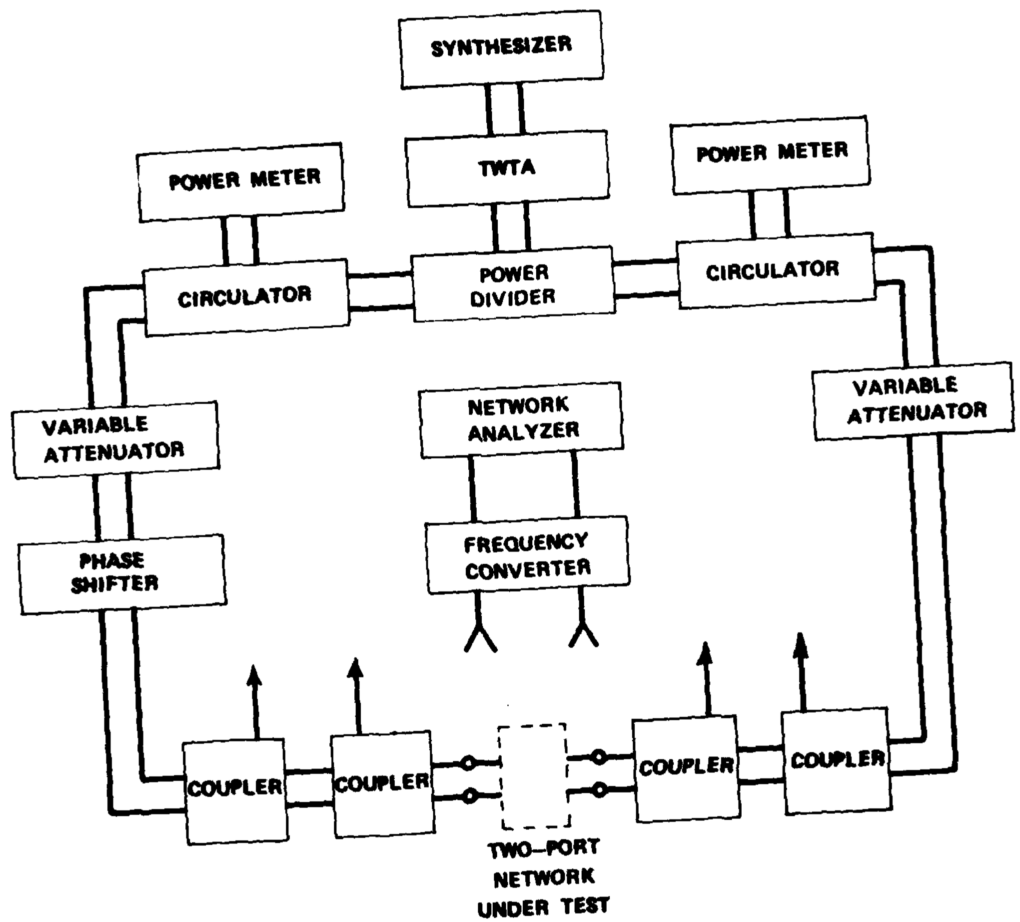
I. CONVENTIONAL ONE-SIGNAL S-PARAMETER MEASUREMENT

- MEASURE S_{11} UNDER LARGE SIGNAL CONDITIONS
- ITERATE TO ESTABLISH DESIRED INPUT LEVEL
- DESIGN MATCHING NETWORK (IMN) FOR FET INPUT



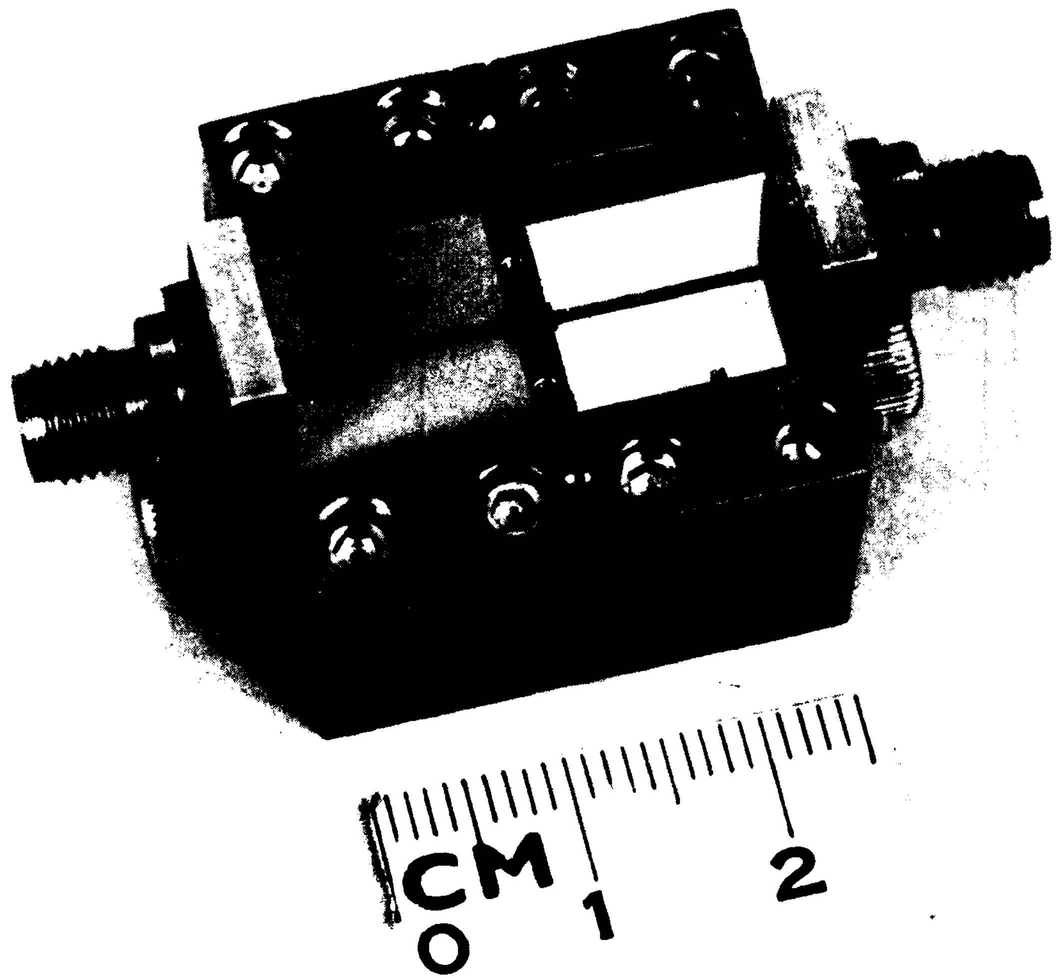
II. TWO-SIGNAL S-PARAMETER MEASUREMENT

- INSTALL IMN AND MEASURE S_{11} TO DETERMINE INPUT MATCH
- MEASURE S_{22} UNDER LARGE SIGNAL CONDITIONS
- DESIGN OUTPUT MATCHING NETWORK

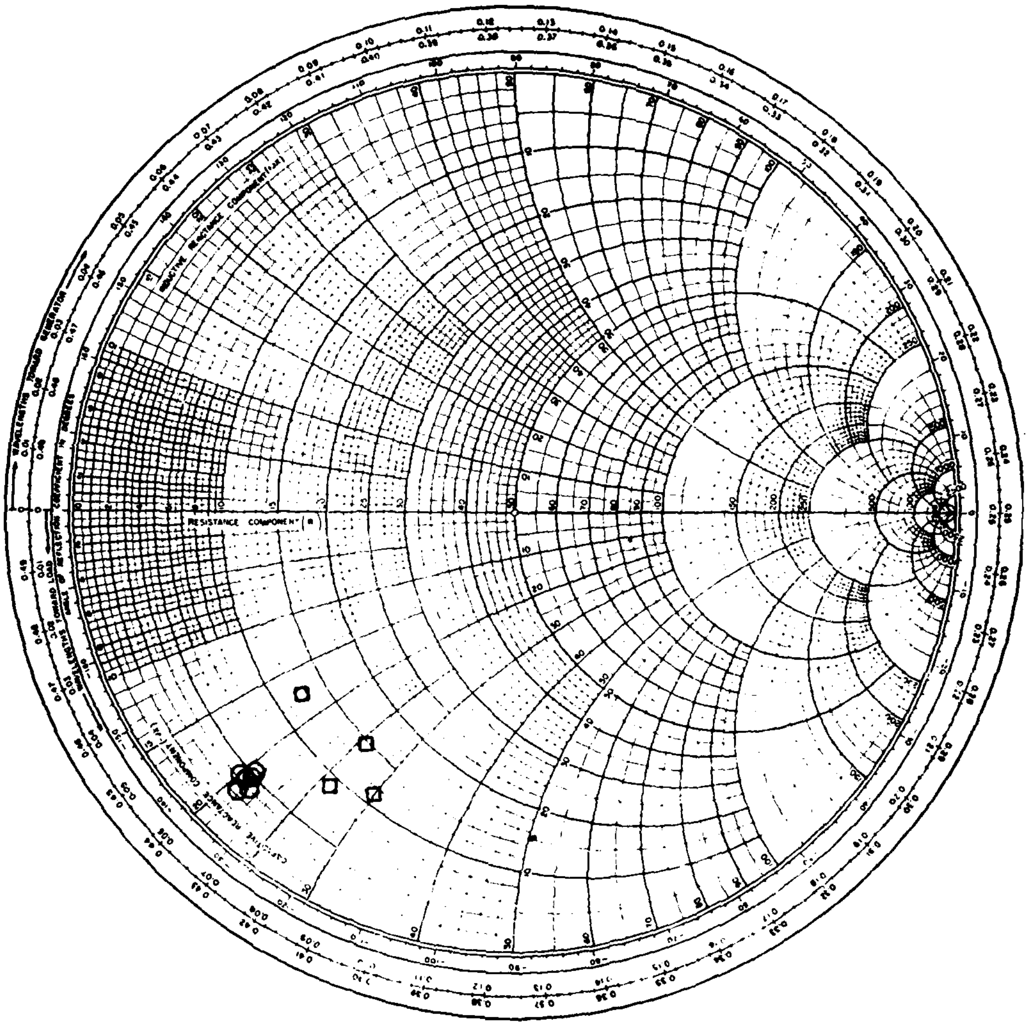


Test Configuration For Two Signal Measurement

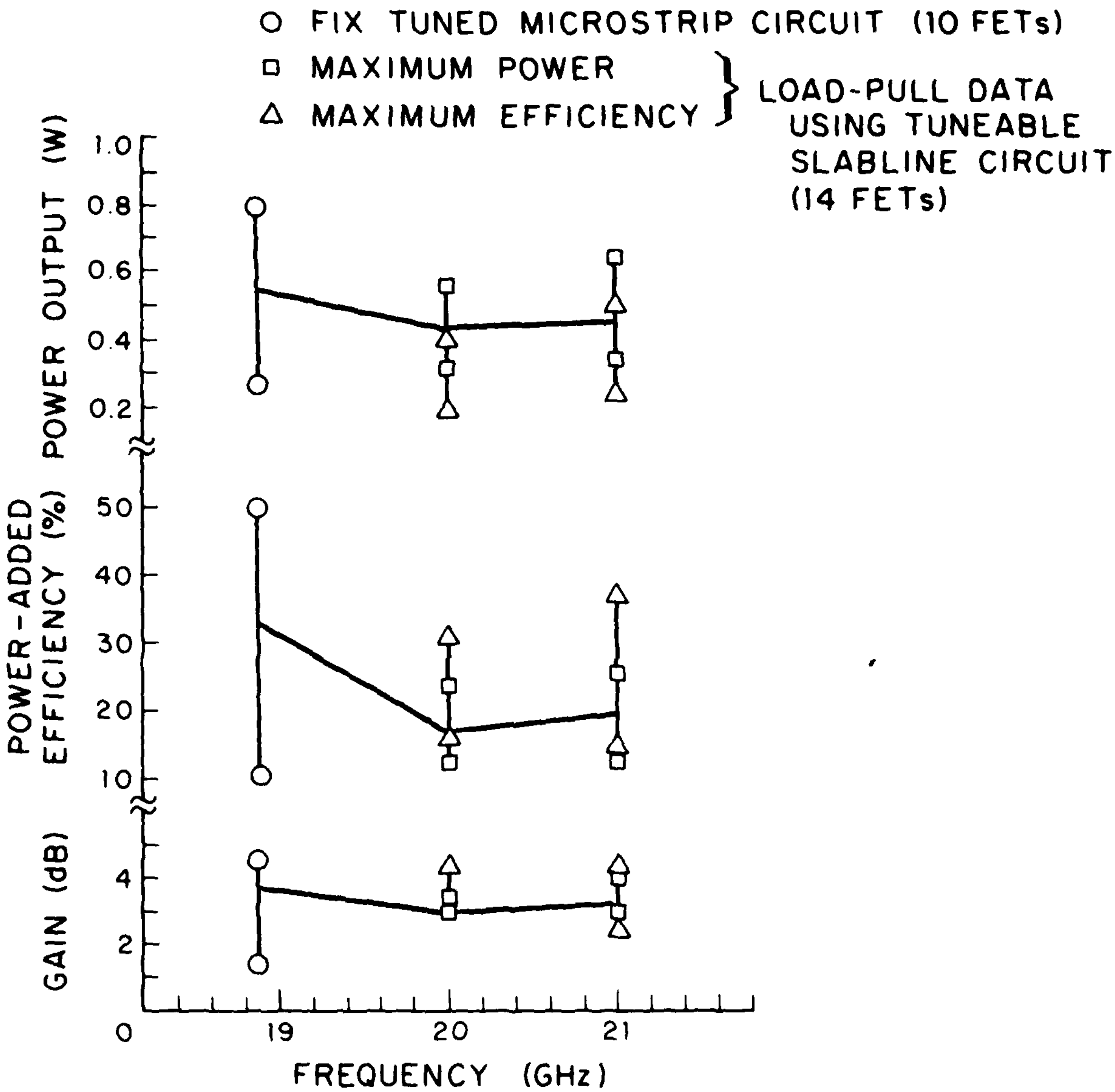
Figure 19.



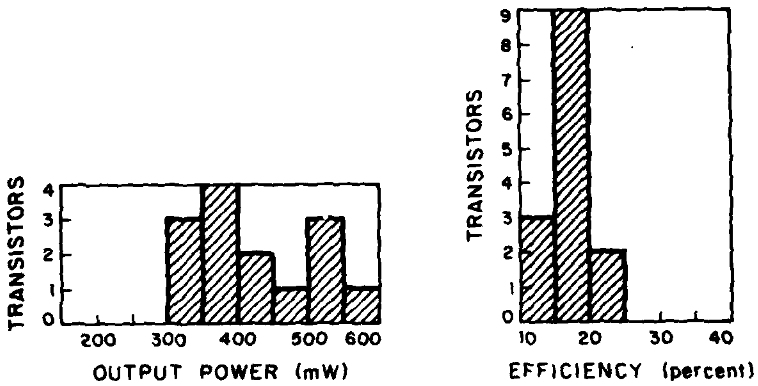
Microstrip Test Fixture



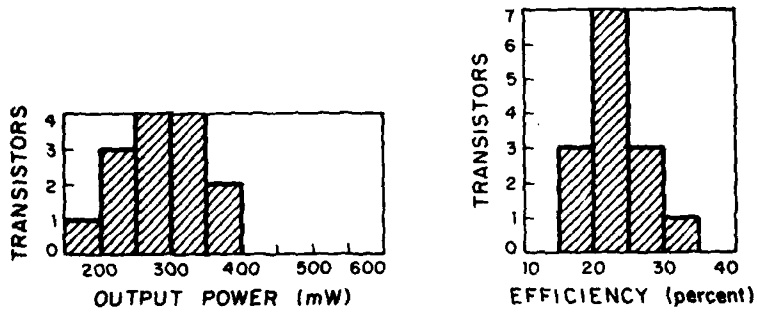
Comparison of Load-Pull and S-Parameter Data.



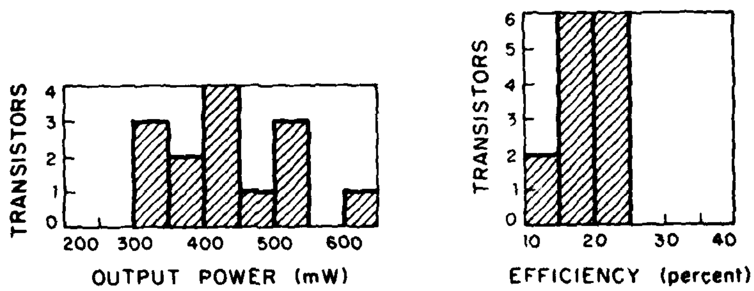
0.5 W FET Performance Versus Frequency.



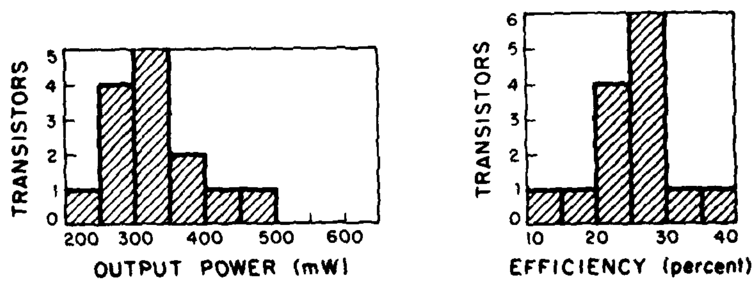
20 GHz Optimum Power Bias and Tuning.



20 GHz Optimum Efficiency Bias and Tuning.

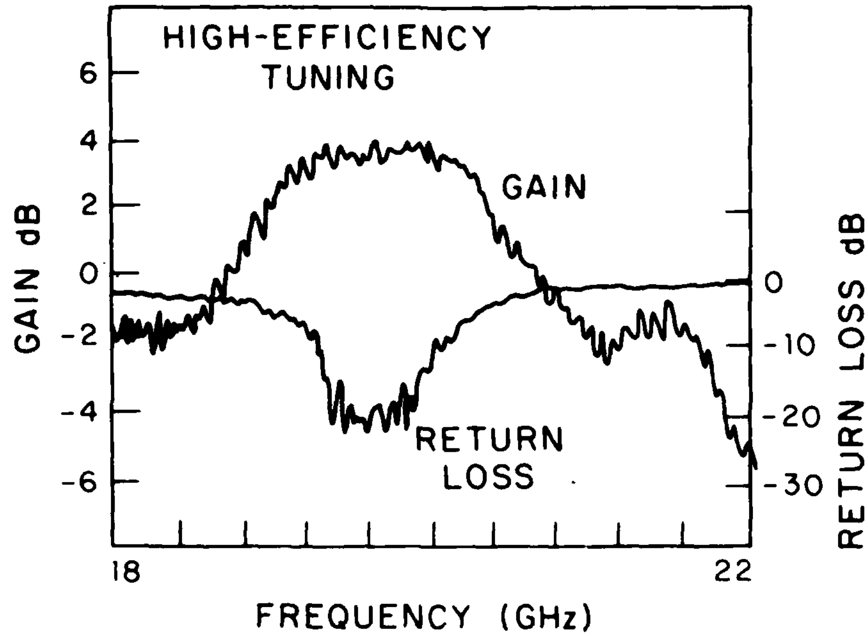


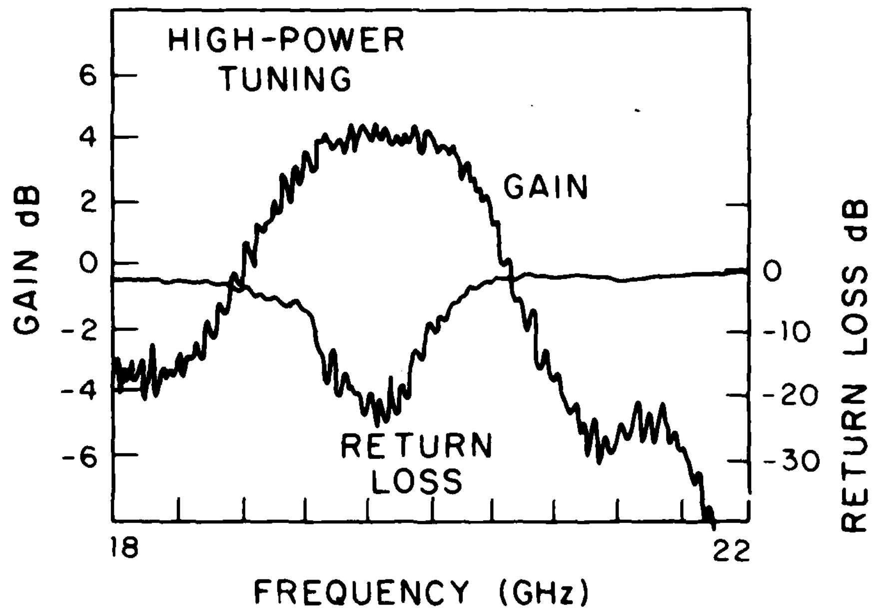
21 GHz Optimum Power Bias and Tuning.



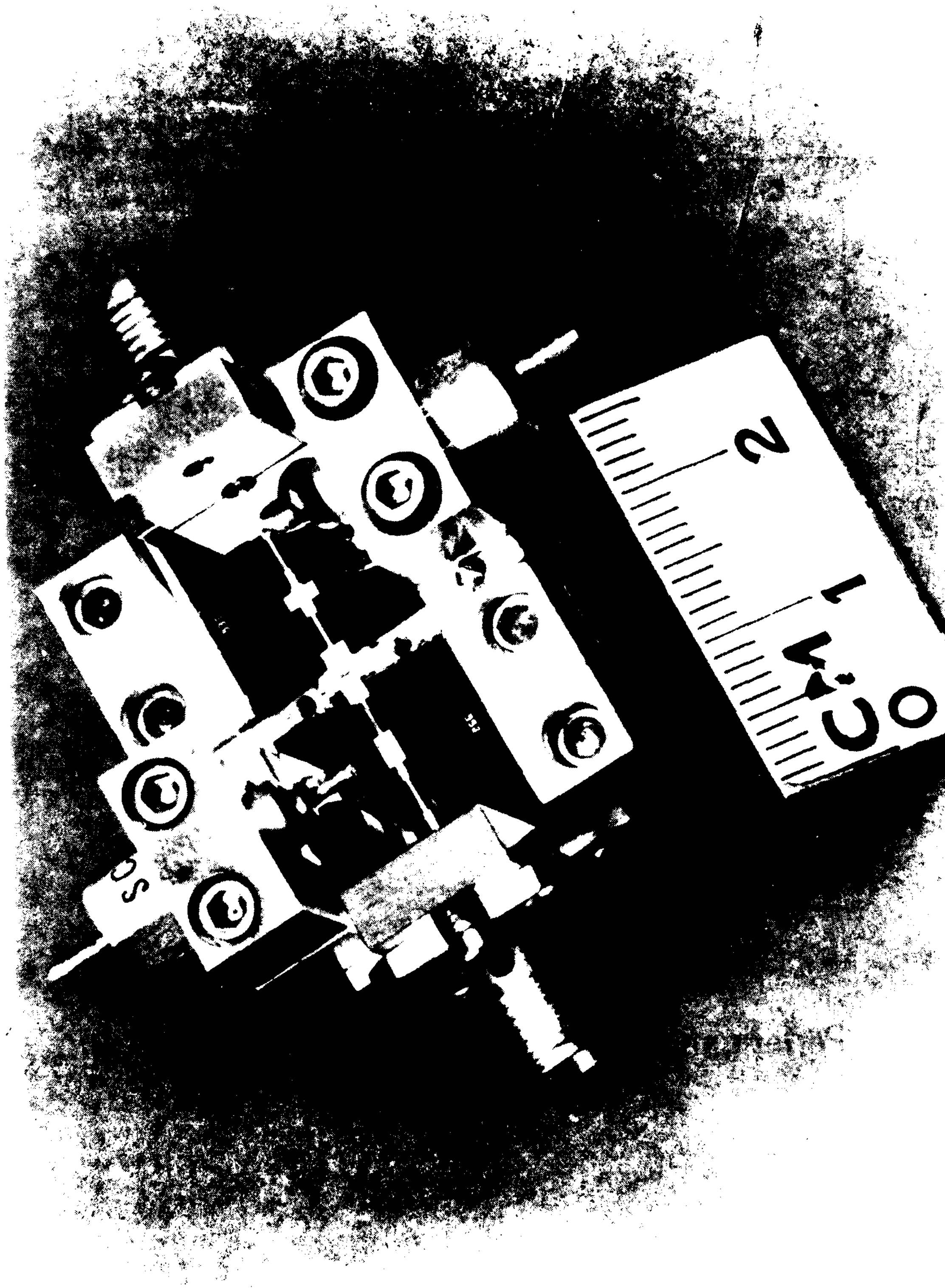
21 GHz Optimum Efficiency Bias and Tuning.

0.5 W Power MESFET Performance Summary.

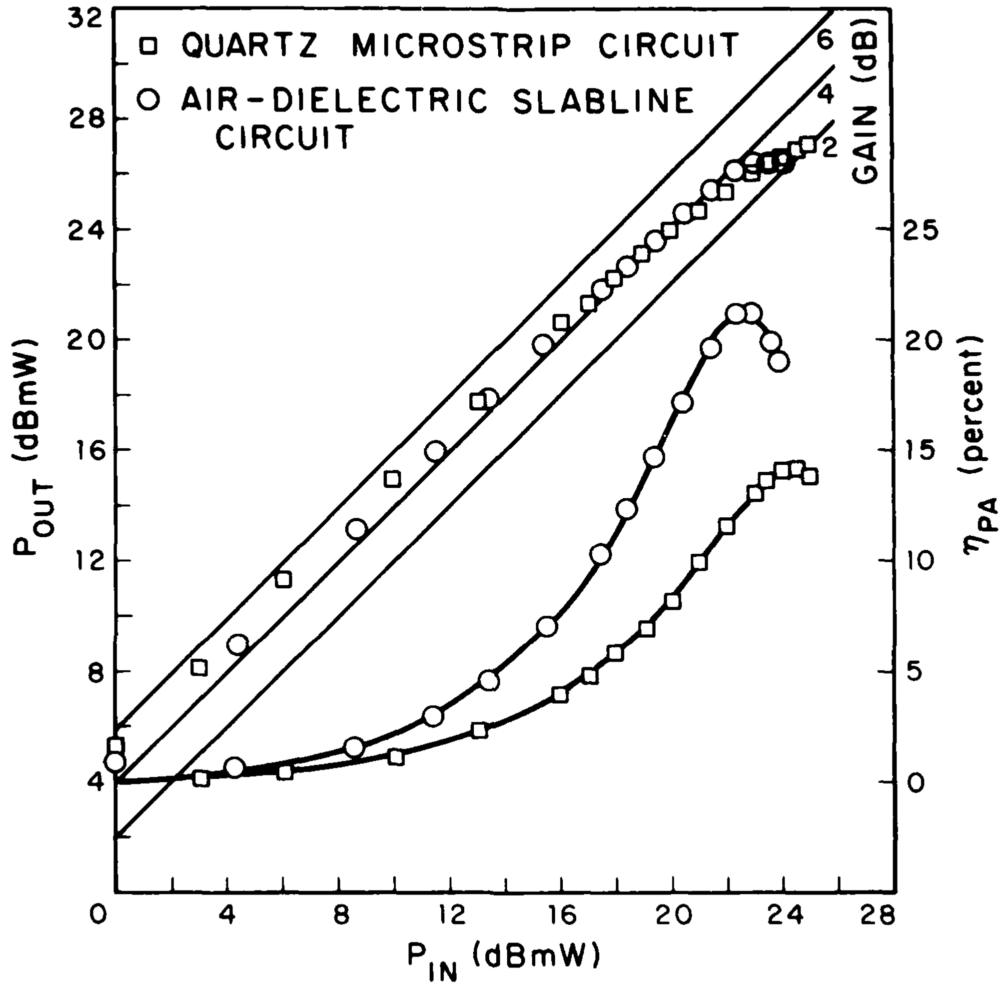




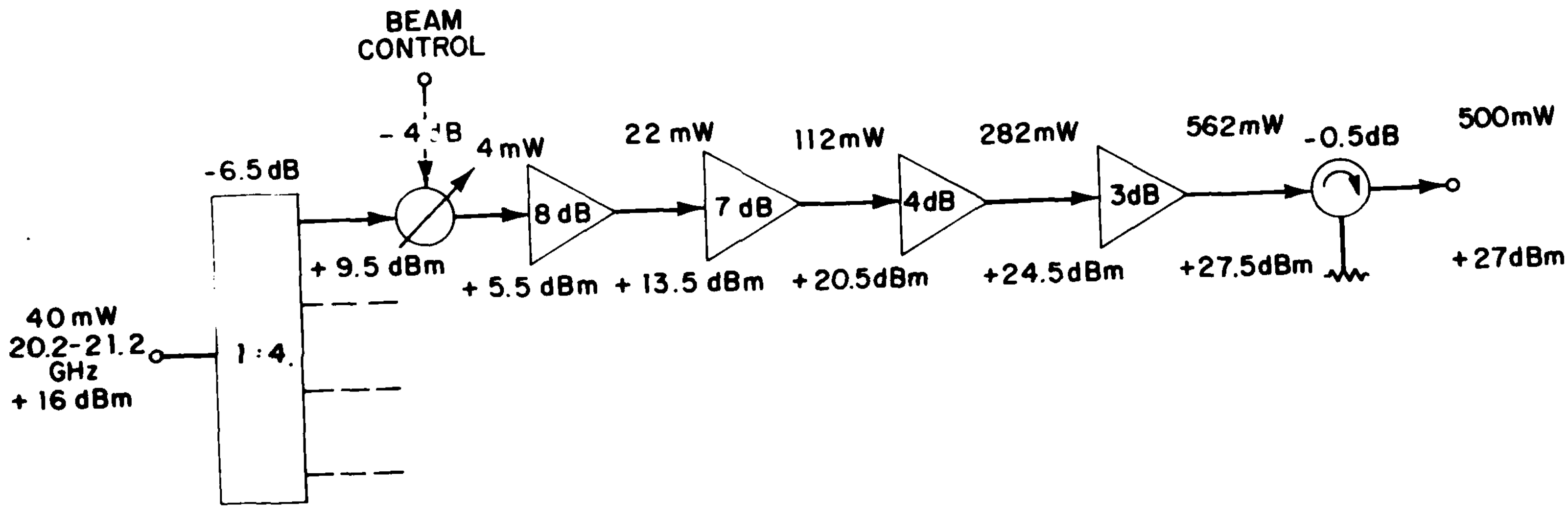
Swept Response of Slabline Amplifier.



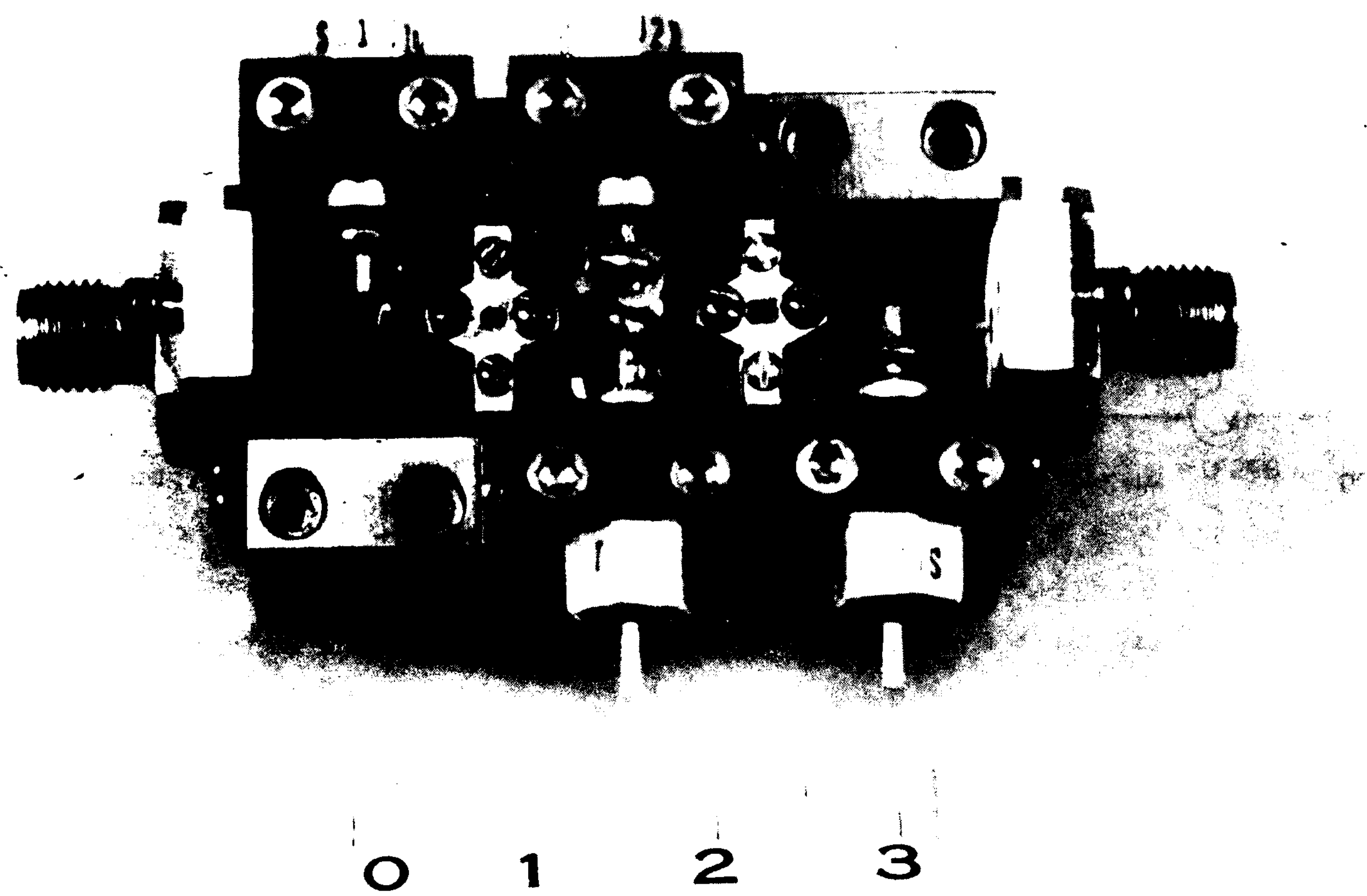
Microstrip Amplifier



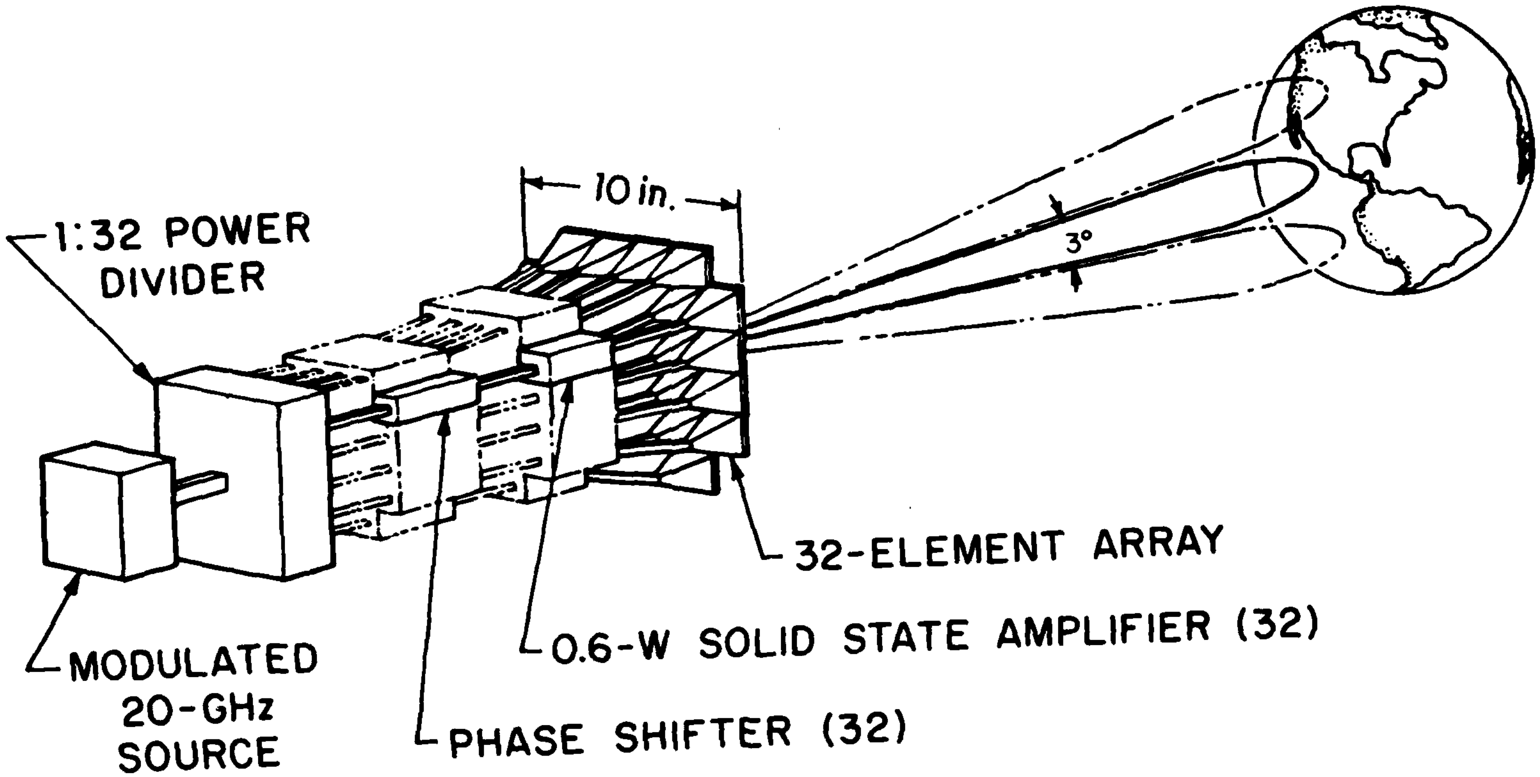
Performance of Slabline and Microstrip Amplifiers.



20 GHz Transmitter Test-Bed.



Two-Stage Microstrip Amplifier



Artist's Conception of a Beam-Hopped Downlink Transmitter.

Conclusion

K–Band Receiver Development

- LOW-NOISE FET CHARACTERIZATION TECHNIQUES
- RIDGE-TRANSFORMER WAVEGUIDE/MICROSTRIP TRANSISTION
- LOW NOISE AMPLIFIER:

  4.5 dB NOISE FIGURE WITH 6 dB OF GAIN

K–Band Transmitter Development

- GaAs POWER MESFETS

  0.5 W POWER OUTPUT AT 20% POWER-ADDED EFFICIENCY

- LARGE SIGNAL FET CHARACTERIZATION TECHNIQUES

  LOAD-PULL/TWO-SIGNAL S-PARAMETERS

- FET PERFORMANCE EVALUATED IN SLABLINE AND MICROSTRIP CIRCUITRY

- COMPLETE AMPLIFIER STAGE

  0.4 W POWER OUTPUT/15% EFFICIENCY/3.0 dB GAIN

Countinuing Developement

- HIGH-GAIN (8 dB) 0.1 W FETS

- HIGH-POWER 1.0 W FETS

DESIGN AND OPTIMIZATION OF LOW NOISE AND POWER FETs FOR EHF APPLICATIONS

Hughes Aircraft

H. Yamasaki

(Document not available)

HIGH PERFORMANCE LOW COST MIXERS
FOR COMMUNICATION APPLICATIONS

HUGHES AIRCRAFT

H. Yamasaki

(Document not available)

IMPATT POWER BUILDING BLOCKS FOR 20 GHz
SPACEBORNE TRANSMIT AMPLIFIER

LNR Communications

H. C. Okean

IMPATT POWER BUILDING BLOCKS FOR 20 GHz

SPACEBORNE TRANSMIT AMPLIFIER

by

J. Asmus, Y. Cho, J. deGruyl, A. Giannakopoulos
and
H.C. Okean

presented at:

EHF SATCOM Technology Workshop
San Diego, California
August, 1981

IMPATT POWER BUILDING BLOCKS FOR 20 GHz

SPACEBORNE TRANSMIT AMPLIFIER*

by

J. Asmus, Y. Cho, J. deGruyl, A. Giannakopoulos
and
H.C. Okean
LNR Communications, Inc.

Single-stage circulator coupled IMPATT "building block" constituents of a 20 GHz solid state power amplifier (SSPA) currently under development for spaceborne downlink transmitter usage has been demonstrated as providing ~1.25 to 1.5W RF power output at 3 to 5 dB operating gain over a 1 GHz bandwidth. Using either commercially available or recently developed in-house GaAs Schottky Read-profile IMPATT diodes, DC/RF power added efficiencies of 11 to 15 percent were achieved. A two stage IMPATT driver amplifier with similar RF output power capability exhibited 13 $\pm$ 0.5 dB operating gain over a 1 GHz bandwidth. A companion 20 GHz FET driver preamplifier is also under development. Extension of the above to the development of a "full-up" 20W IMPATT transmitter is currently in progress.

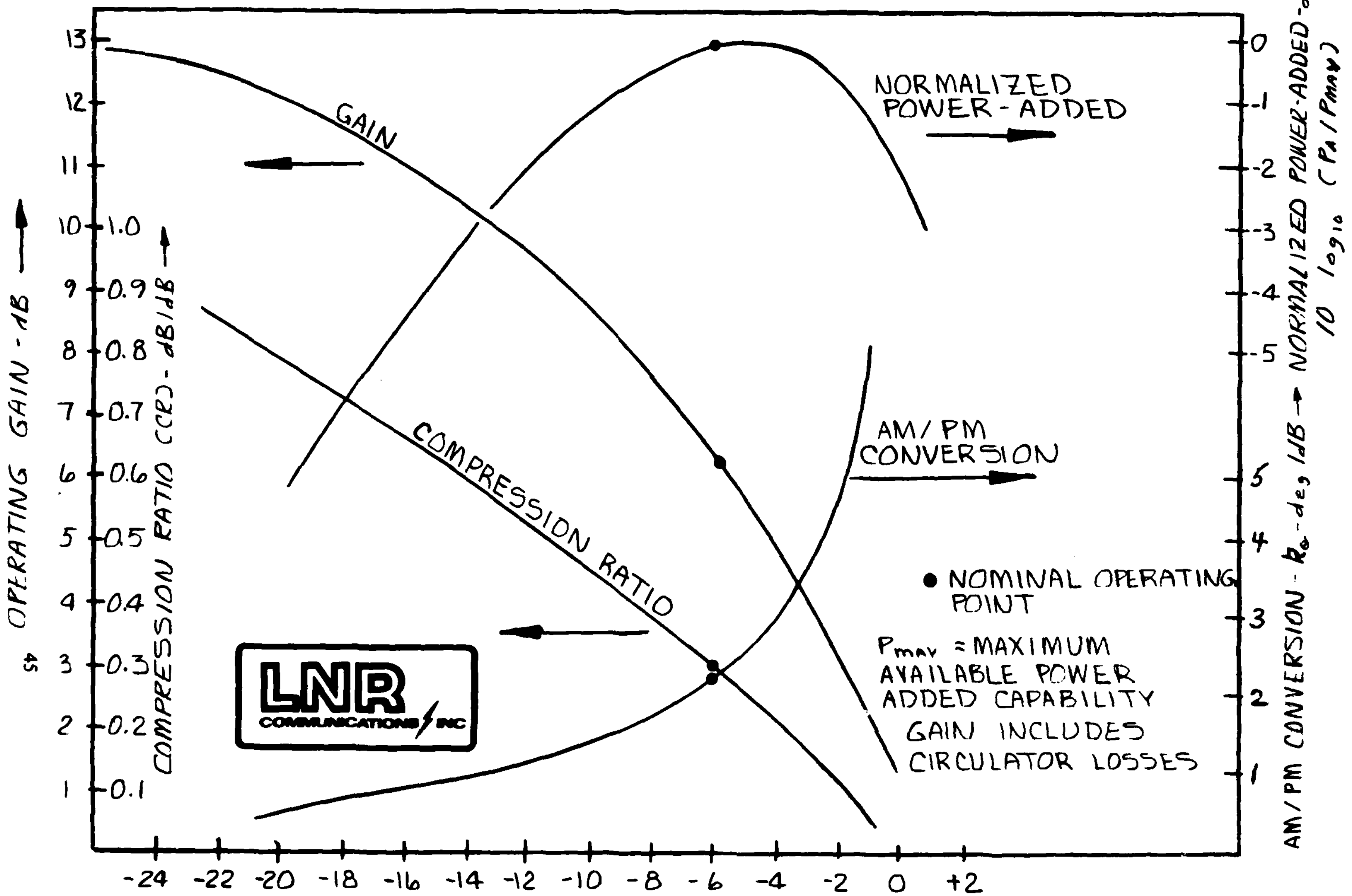
---

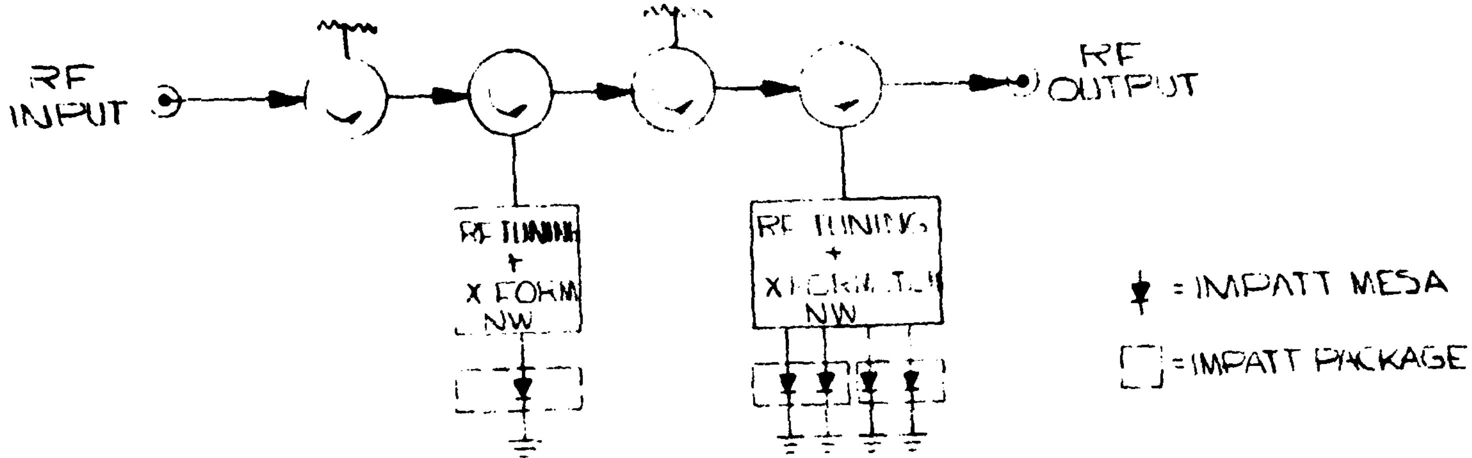
*This effort is sponsored in part by NASA Lewis Research Center and the Air Force Avionics Laboratory under Contracts No. NAS3-22491 and F33615-80C-1182, respectively.

20 GHz SOLID STATE TRANSMITTER DESIGN OBJECTIVES

PARAMETRIC	DESIGN OBJECTIVE (OVER PASSBAND)
INPUT SIGNAL FORMAT	ANGLE MODULATED, SINGLE CARRIER
CENTER FREQUENCY	20 GHz
RF BANDWIDTH	1.0 GHz
SATURATED RF OUTPUT POWER	20 WATTS (MIN)
RF POWER OUTPUT VARIATION WITH FREQUENCY AND TEMPERATURE	0.6DB(P-P) @ NOMINAL DRIVE LEVEL 1.2DB(P-P) OVER NOMINAL $\pm$2DB DRIVE LEVEL RANGE
RF GAIN @ SATURATION	30 DB (MIN)
IN BAND OVERDRIVE SURVIVABILITY	5 DB ABOVE NOMINAL INPUT LEVEL
GAIN SLOPE	0.1 DB/MHz (MAX)
INPUT VSWR	1.25:1 (MAX)
OUTPUT VSWR	1.5:1 (MAX)
GROUP DELAY VARIATION	0.5 nS P-P (MAX) OVER 50 MHz SLOT
AM/PM CONVERSION	6°/DB (MAX)
DEVIATION FROM PHASE LINEARITY	10° (MAX)
SPURIOUS RESPONSE (SUM OF HARMONIC COMPONENTS)	17 DB BELOW CARRIER
SPURIOUS RESPONSE (NON-HARMONIC COMPONENTS)	60 DB BELOW CARRIER/20 MHz BAND
NOISE FIGURE	25 DB (MAX)
DC-RF EFFICIENCY	15 PERCENT (MIN)
PRIME DC VOLTAGE INPUT	28 V (NOM)
BASEPLATE TEMPERATURE	0 TO 50°C

TRANSFER CHARACTERISTICS OF "BUILDING BLOCK" IMPATT AMPLIFIER STAGE

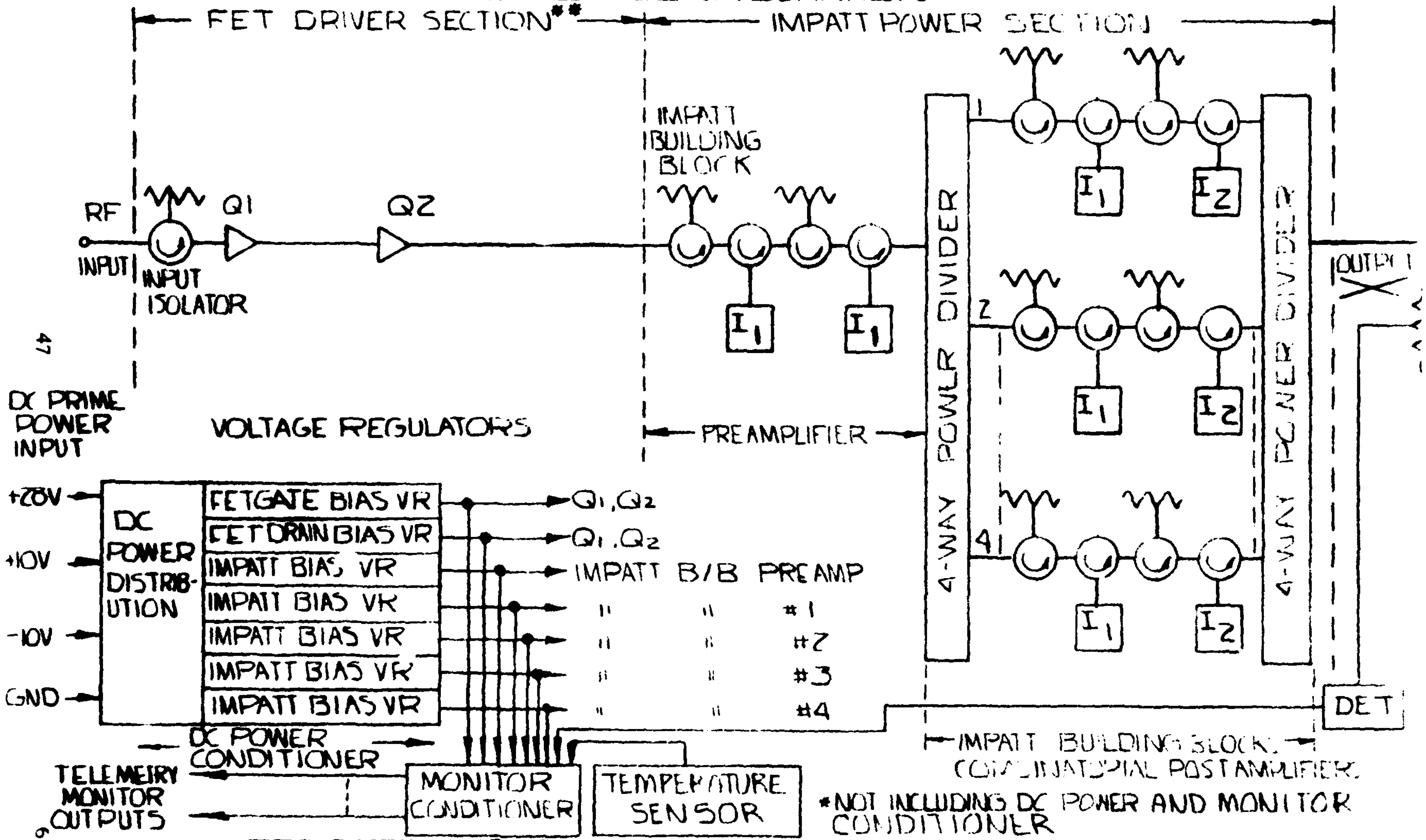




PROJECTED PERFORMANCE	PREAMP	COMBINATORIAL POSTAMP
. FREQUENCY RANGE:	-----19.5-20.5 GHz------	
. RF OUTPUT LEVEL:	1.56W	6.25W
. RF INPUT LEVEL:	0.02W	0.36W
. OPERATING GAIN:	18.9dB	12.3dB
. DC POWER CONSUMPTION:	10W	25W
. RF/DC POWER-ADDED EFFICIENCY:	15.4%	23.5%
. GAIN COMPRESSION RATIO:	0.18dB/dB	0.09dB/dB
. AM/PM CONVERSION:	2.5 deg/d	3.4 deg/dB
. NOISE FIGURE:	30.5dB	32.5dB
GAIN FLATNESS:	±0.3dB	±0.2dB
PHASE LINEARITY:	±3 deg	±2 deg

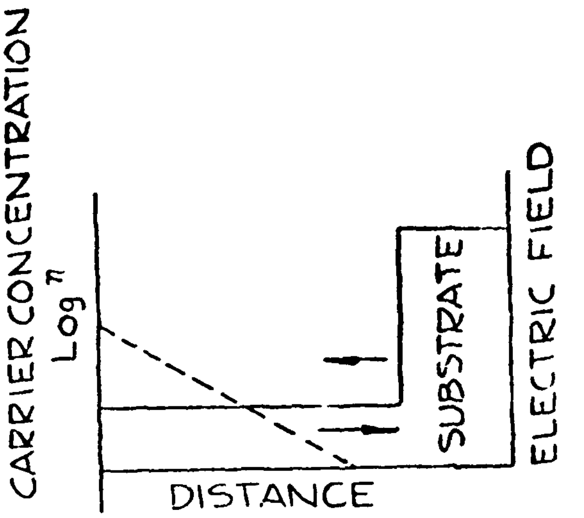
PREFERRED 20 GHz IMPATT POWER SECTION
"BUILDING BLOCK" AMPLIFIER DESIGN

PREFERRED 20 GHz TRANSMITTER AMPLIFIER CONFIGURATION

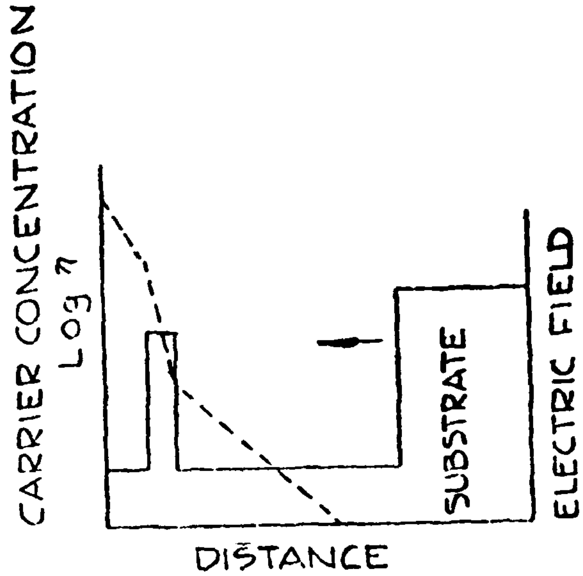


PROJECTED CHARACTERISTICS

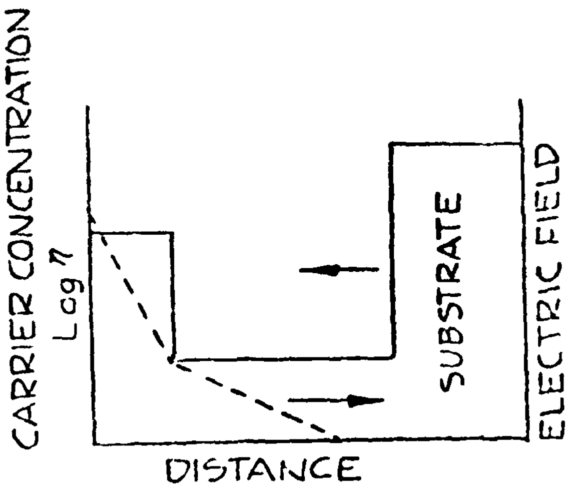
- RF OUTPUT LEVEL: 22.5 W (MIN)
- RF INPUT LEVEL: 2.7 W (NOM)
- OPERATING GAIN: 39.3 dB (NOM)
- DC PRIME POWER: 120 W (MAX)*
- POWER-ADDED EFFICIENCY: 20.4 PERCENT (MIN)*
- GAIN COMPRESSION: 0.016 dB/dB (MAX)
- AM/PM CONVERSION: 5.9 DEG/dB (MAX)
- NOISE FIGURE: 22.5 dB (NOM)



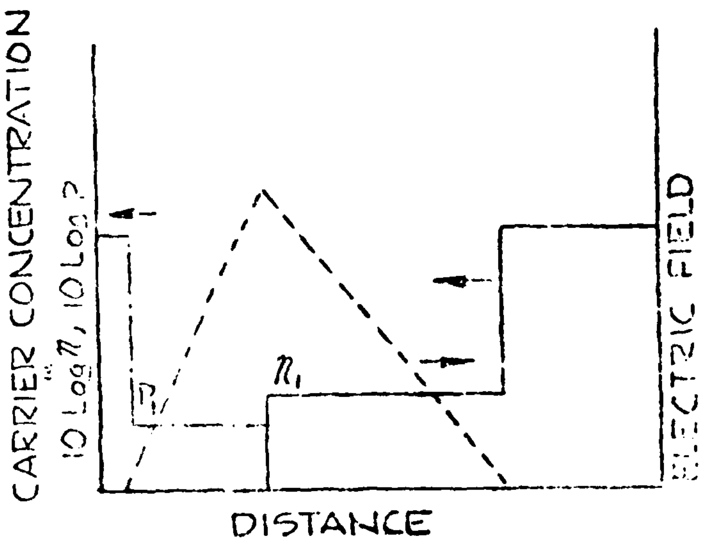
A. SDR FLAT DOPING PROFILE



C. SDR LHL DOPING PROFILE
(MODIFIED READ)

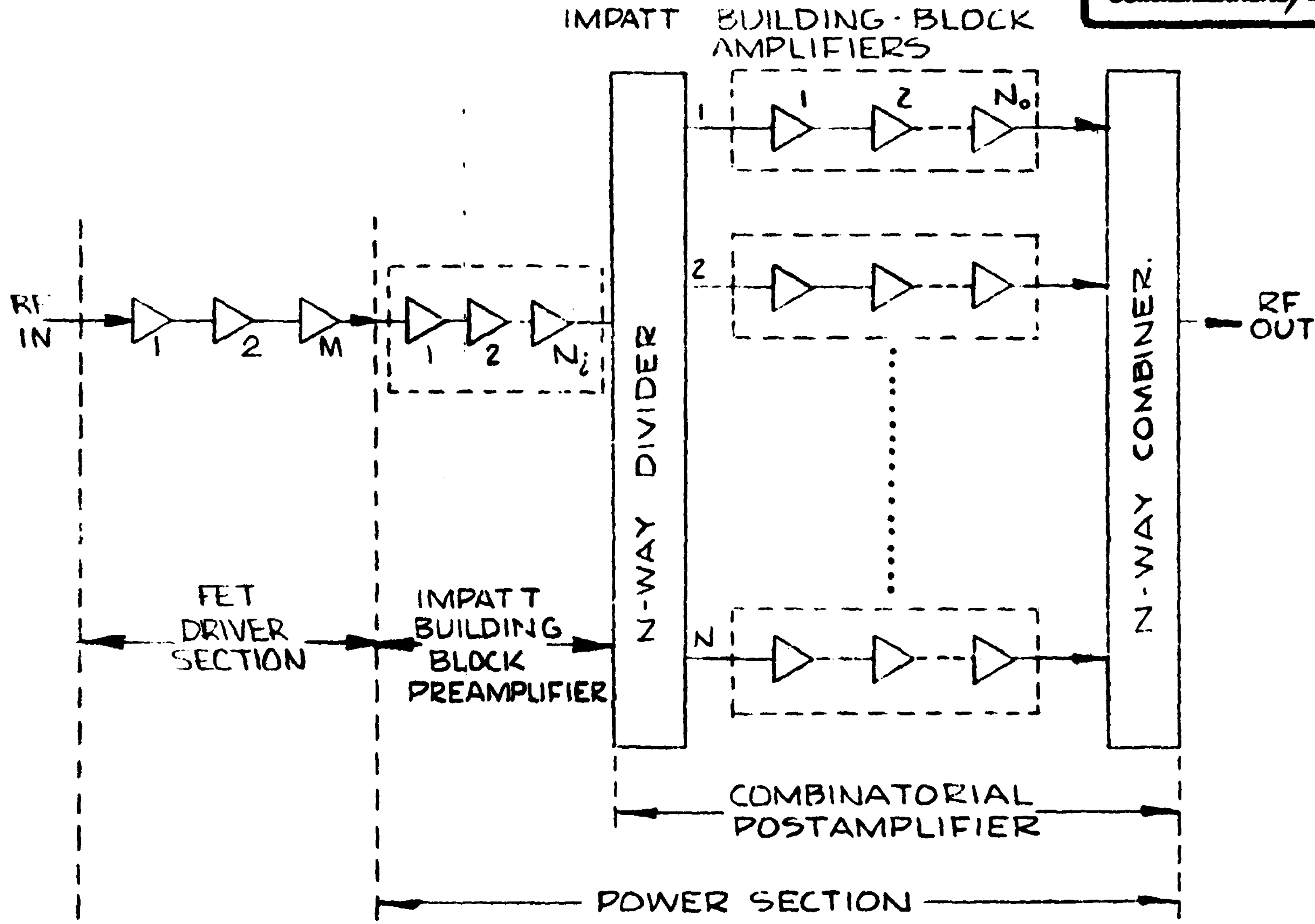


B. SDR HI-LO PROFILE
(MODIFIED READ)

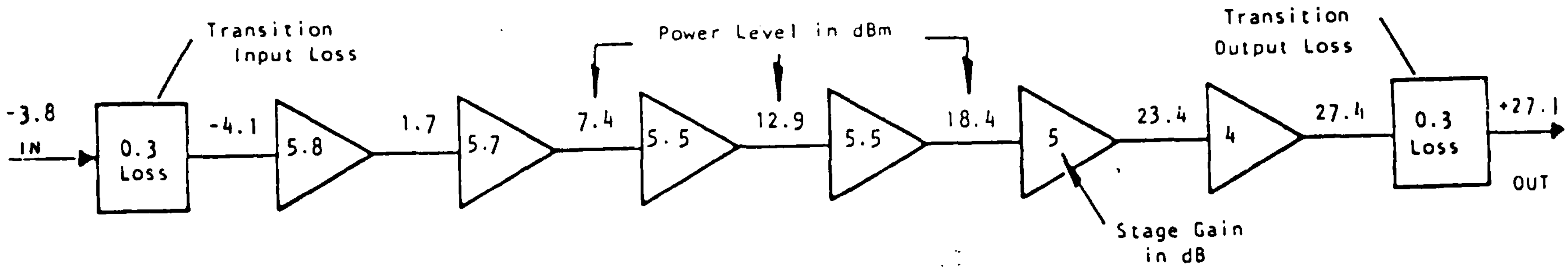


D. DDR FLAT PROFILE

ALTERNATIVE IMPATT DIODE DOPING PROFILES



FUNCTIONAL RF TOPOLOGY OF 20GHz IMPATT TRANSMITTER



Gain Stage	1	2	3	4	5	6
Gate Width (μm)	150	150	300	600	1350	2x1350
Current (mA)	30	30	60	120	250	500
Voltage (V)	7	7	7	7	7	7
Efficiency (%)	0.5	1.9	3.3	5.9	8.5	9.4

Total Module Gain - 30.9 dB
Module Output Power - 513 mW
DC Input Power - 6.93 W
Module Efficiency - 7.4%

Modified Block Diagram of 31 dB Amplifier Module Including Bias Schedule

(Linear Amplifier)

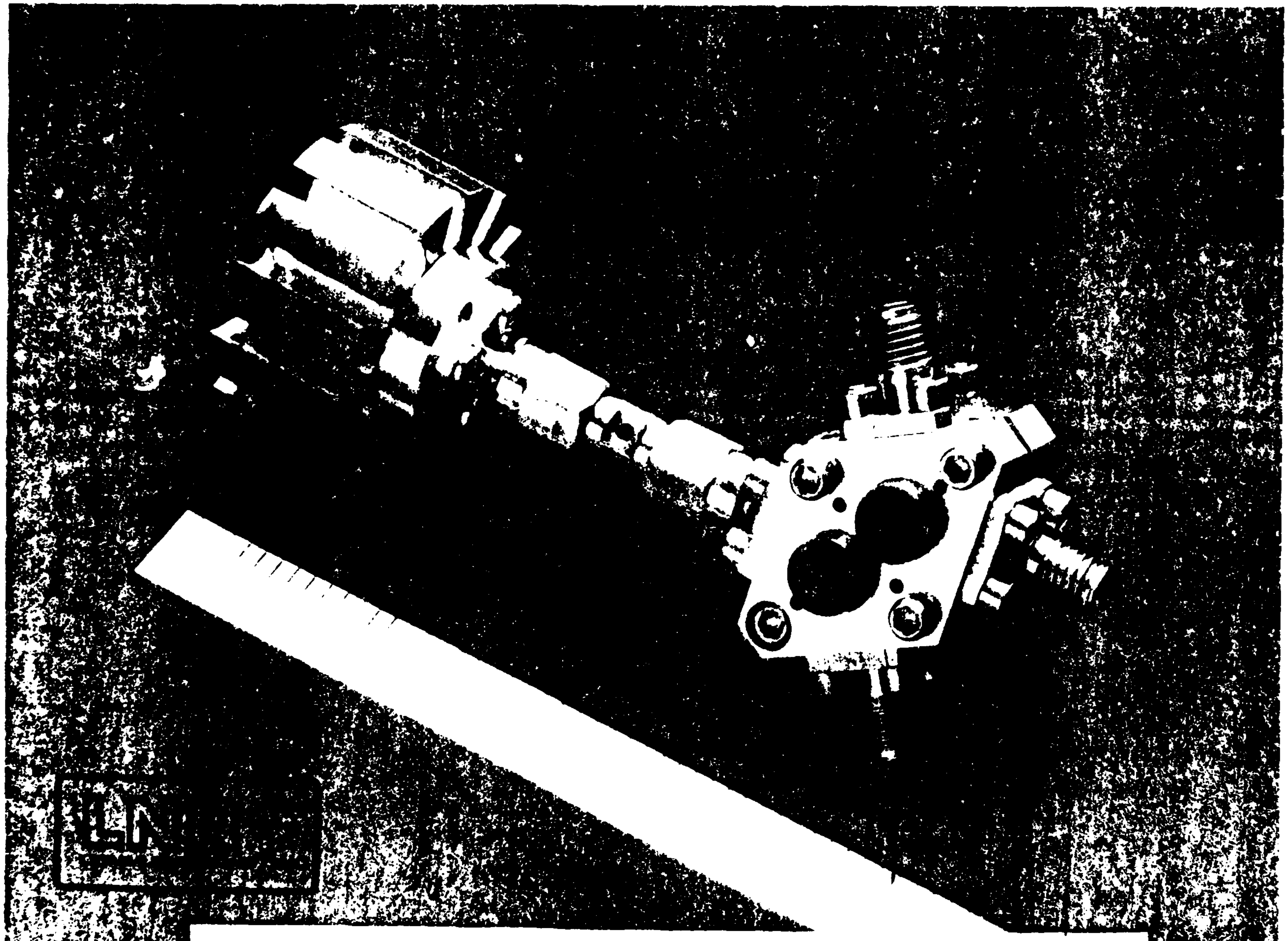
IN-HOUSE K-BAND IMPATT DIODE DEVELOPMENT STATUS

1) TYPE:

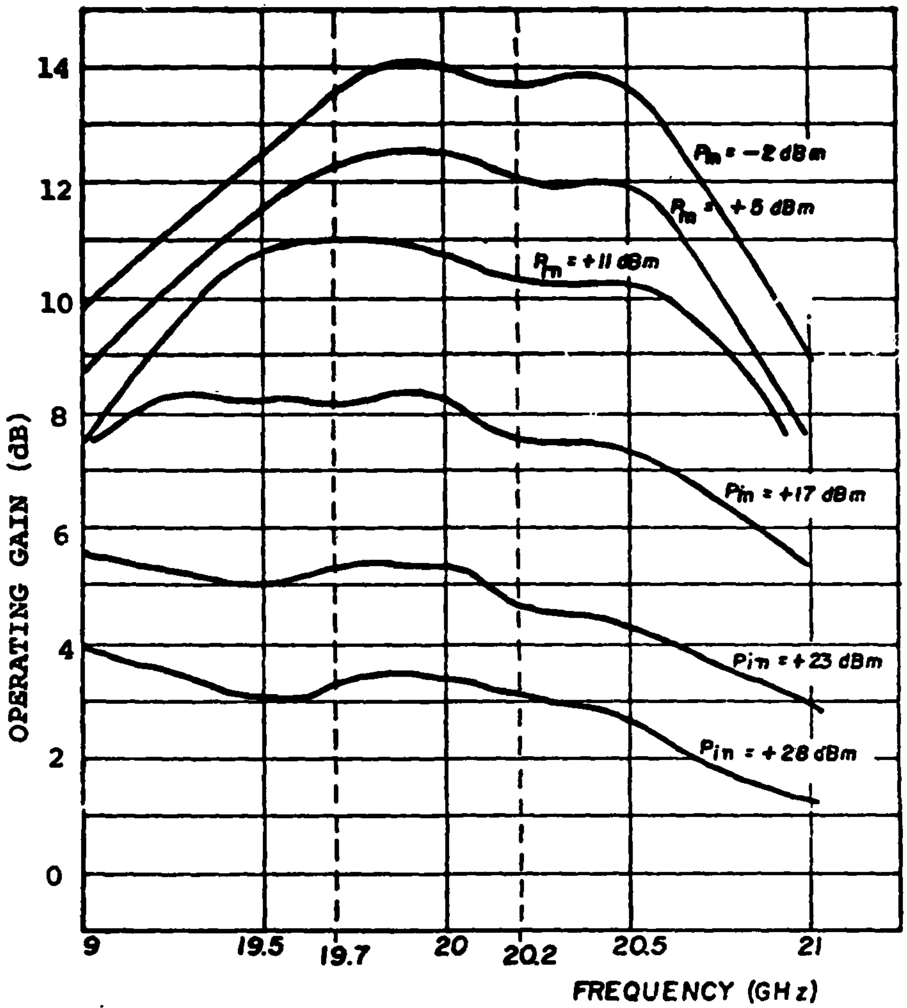
- GaAs MODIFIED READ-PROFILE (LHL)
- SINGLE DRIFT

2) SUMMARY OF RESULTS TO DATE

• FREQUENCY GHz	16-18	18-20
• RF POWER OUTPUT-W (TEST OSC.)	1.5-3.0	1.25-1.75
• DC/RF EFFICIENCY-PERCENT	15-20	10-15
• THERMAL RESISTANCE $^{\circ}C/W$	20	20-22

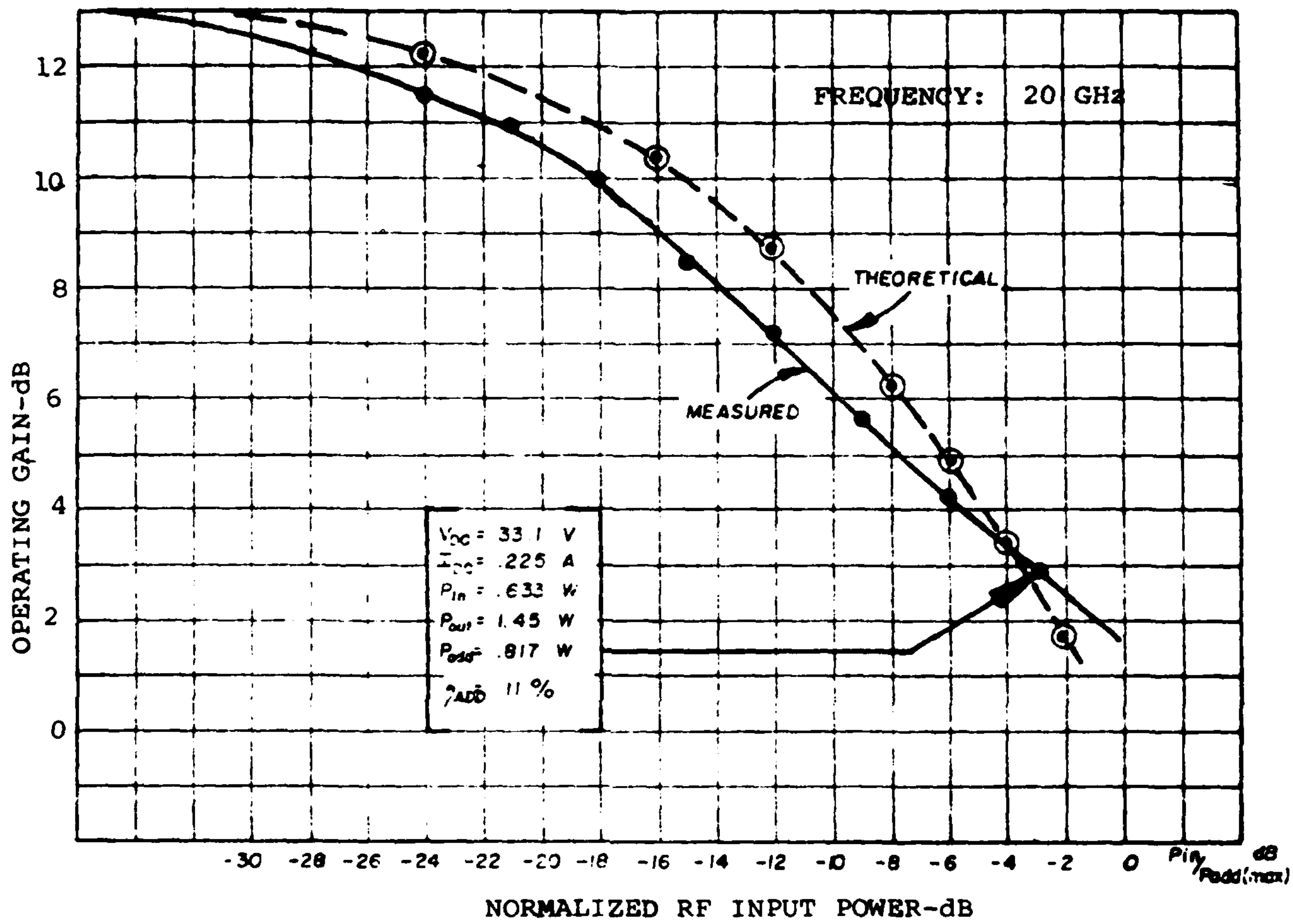


SINGLE STAGE K-BAND IMPATT TEST AMPLIFIER



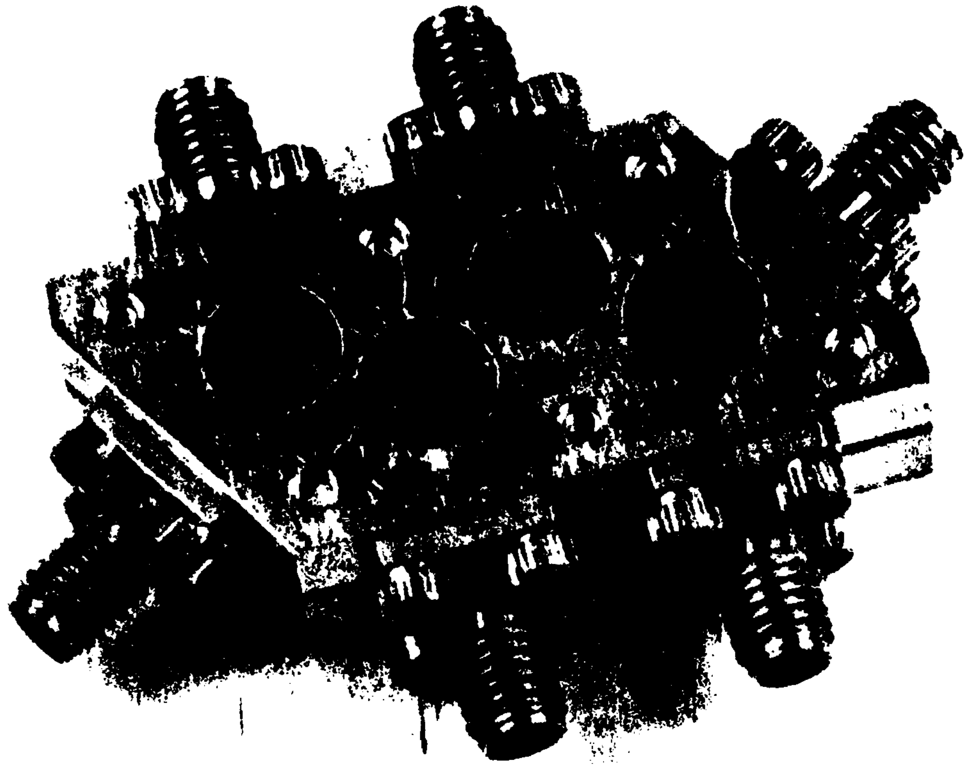
MEASURED GAIN OF SINGLE-STAGE IMPATT AMPLIFIER
UTILIZING LNR IMPATT DIODE

LNR COMMUNICATIONS, INC

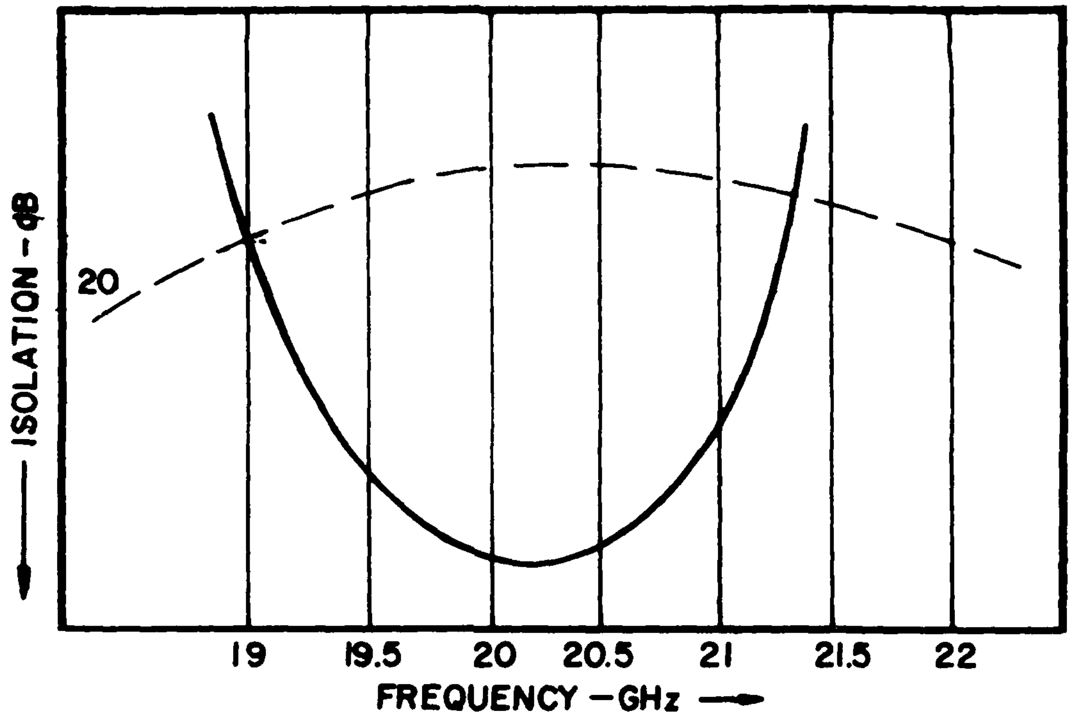


RF TRANSFER CHARACTERISTIC OF SINGLE-STAGE
AMPLIFIER UTILIZING LNR IMPATT DIODE

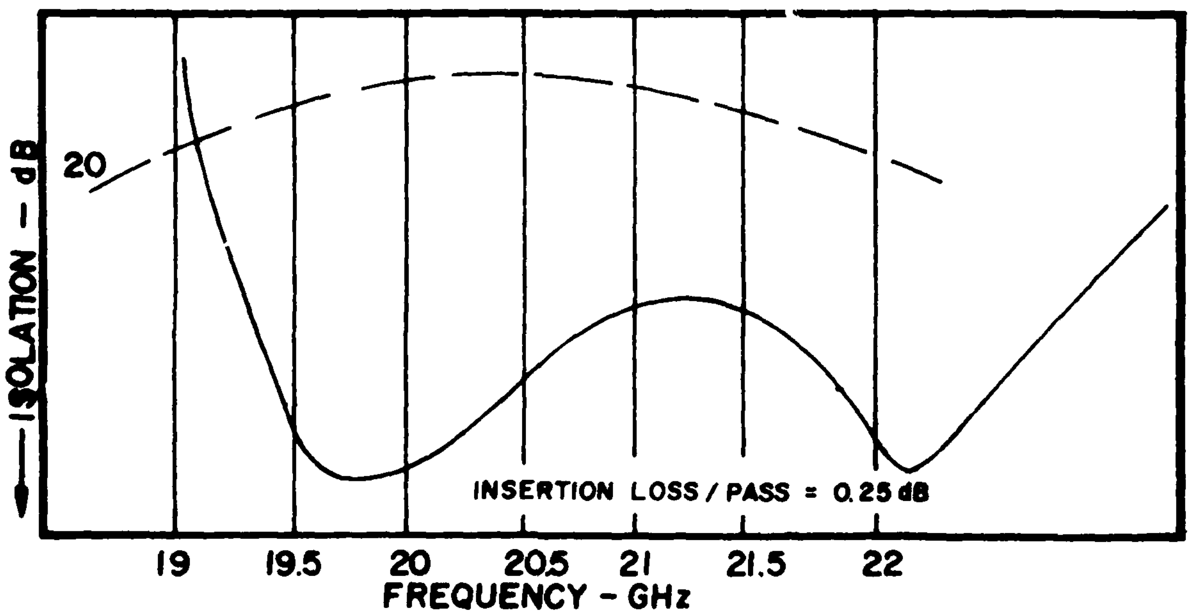
LNR COMMUNICATIONS, INC.



K-BAND 6-PORT STRIPLINE CIRCULATOR

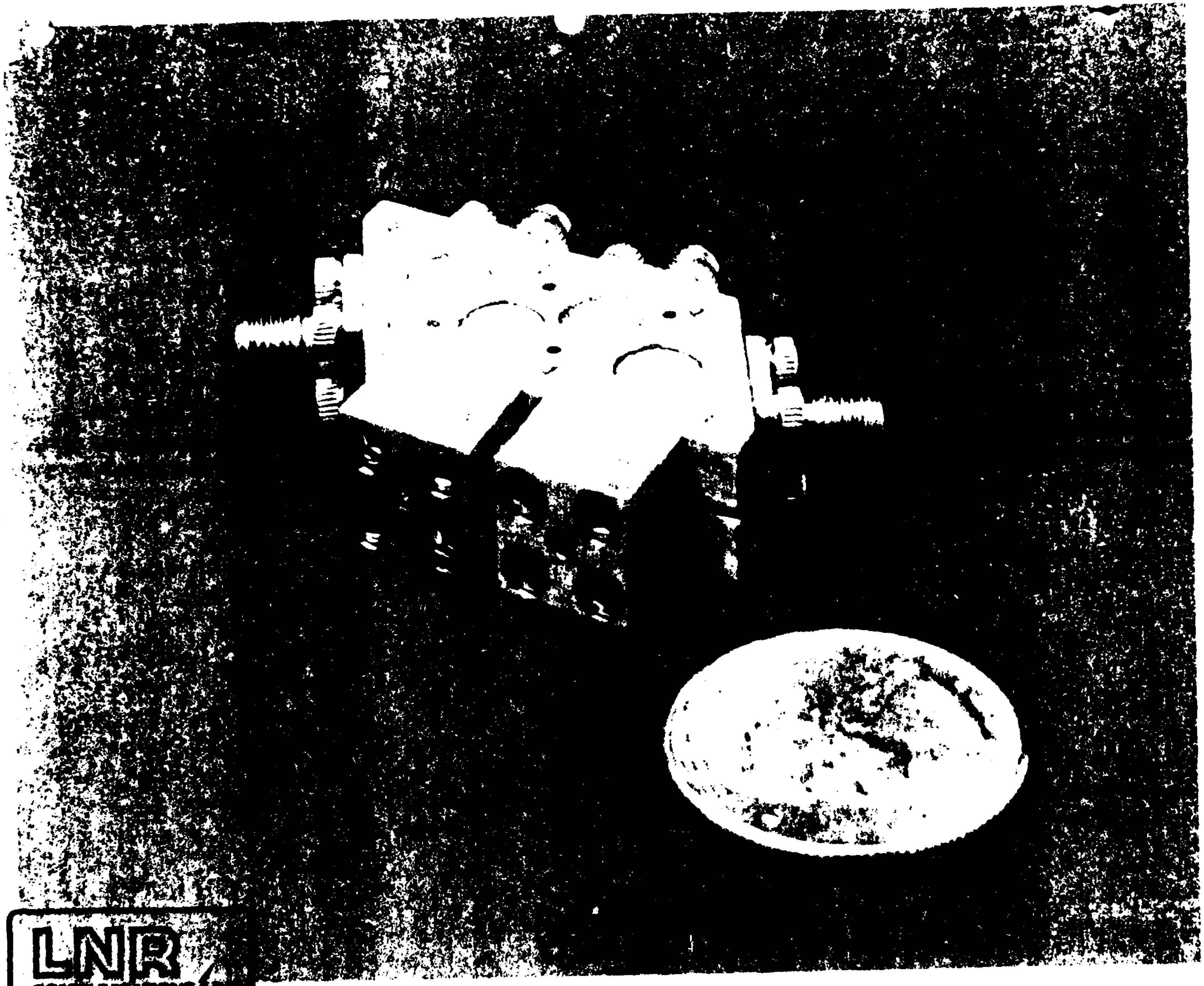


TYPICAL EXTERNAL PORT ISOLATION OF BREADBOARD K-BAND 6-PORT CIRCULATOR

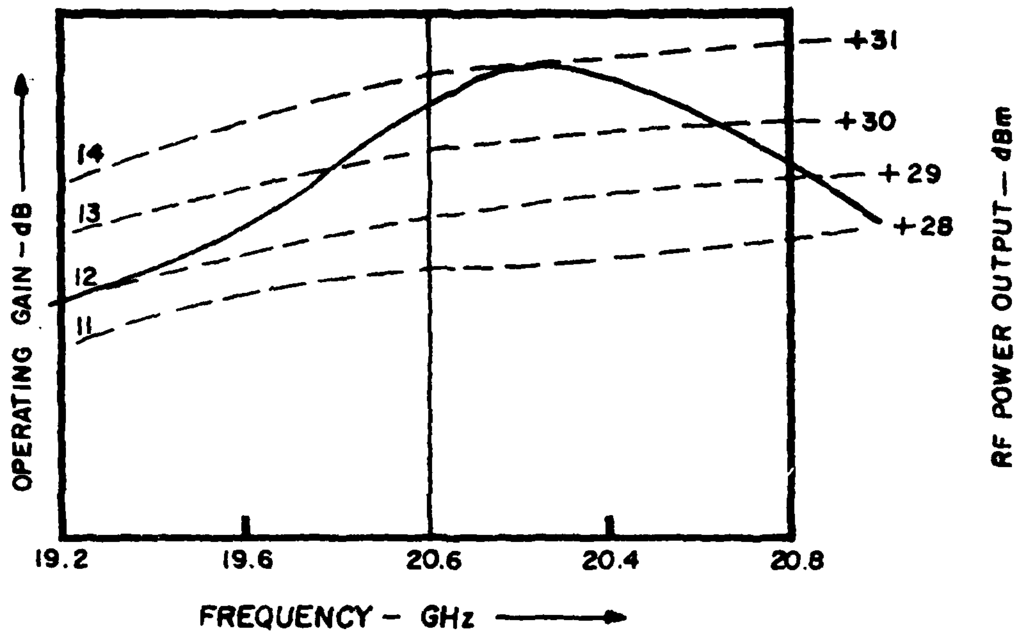


TYPICAL INTERJUNCTION ISOLATION OF BREADBOARD K-BAND 6-PORT CIRCULATOR

LNR COMMUNICATIONS, INC



INTEGRATED TWO-STAGE K-BAND IMPATT AMPLIFIER



INPUT DRIVE LEVEL : + 17 dBm

OPERATING GAIN COMPRESSION RATIO : 0.2 dB/dB

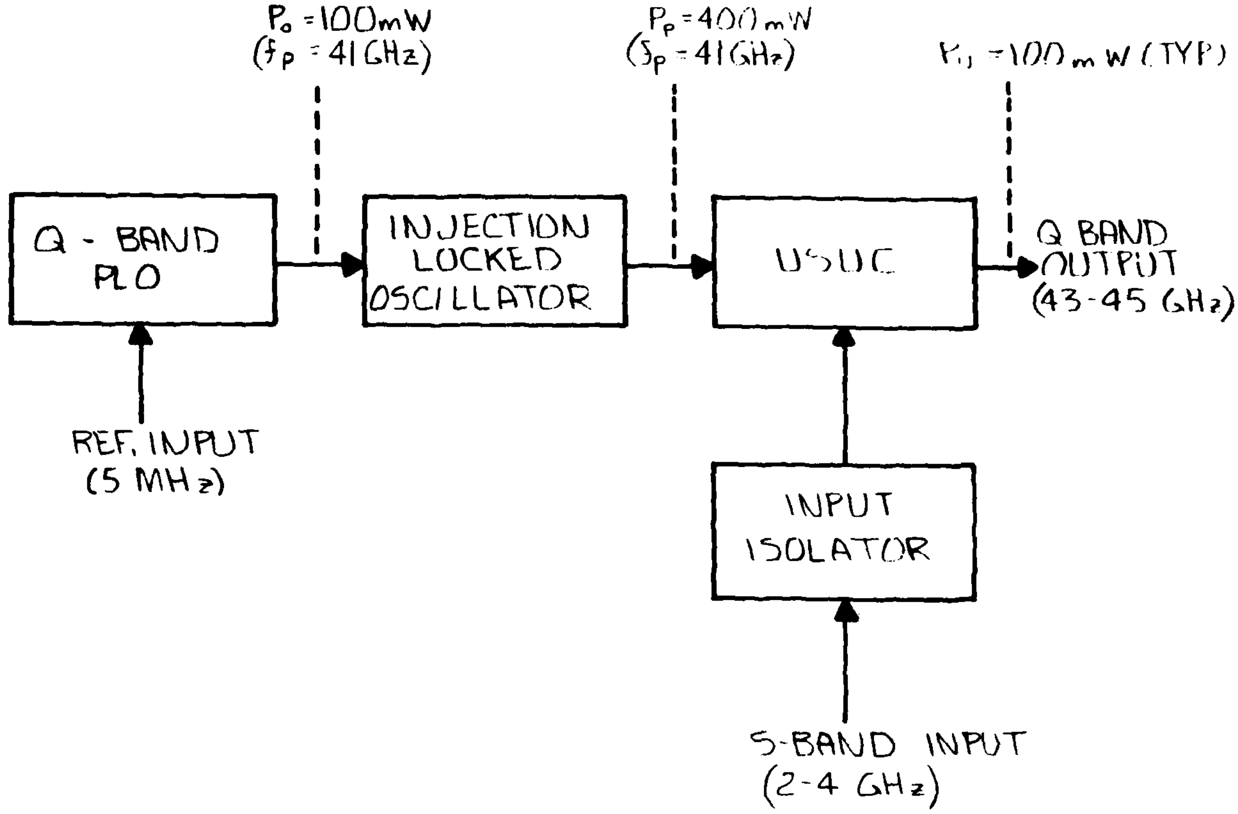
IMPATT DEVICE✦POWER ADDED EFFICIENCY : 18 % (MAX)

DC POWER / STAGE : 6 W

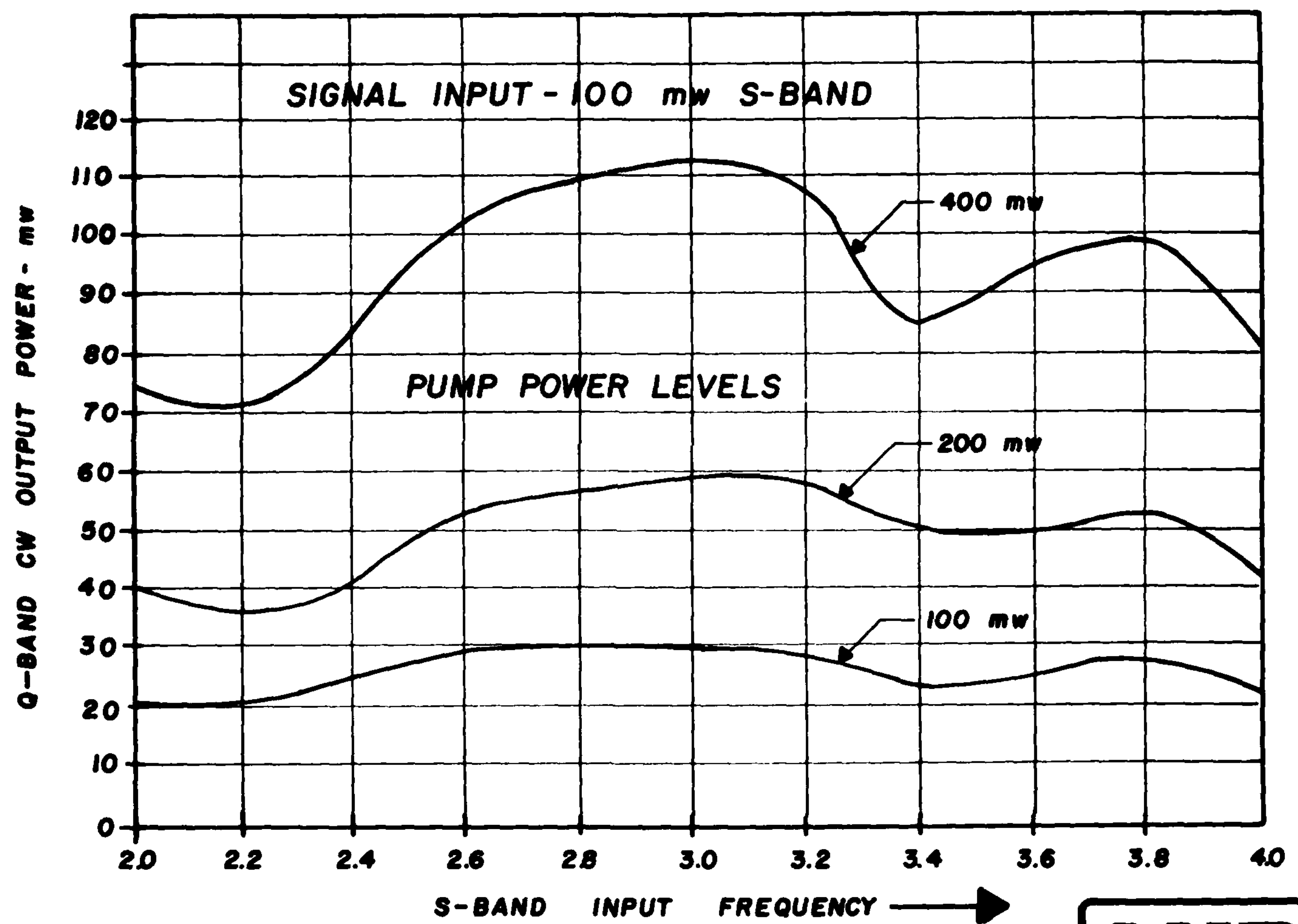
(✦ COMM. AVAIL.)

MEASURED PERFORMANCE
OF
TWO-STAGE IMPATT PREAMPLIFIER

LNR COMMUNICATIONS INC



FUNCTIONAL BLOCK DIAGRAM OF S/Q BAND POWER UPCONVERTER



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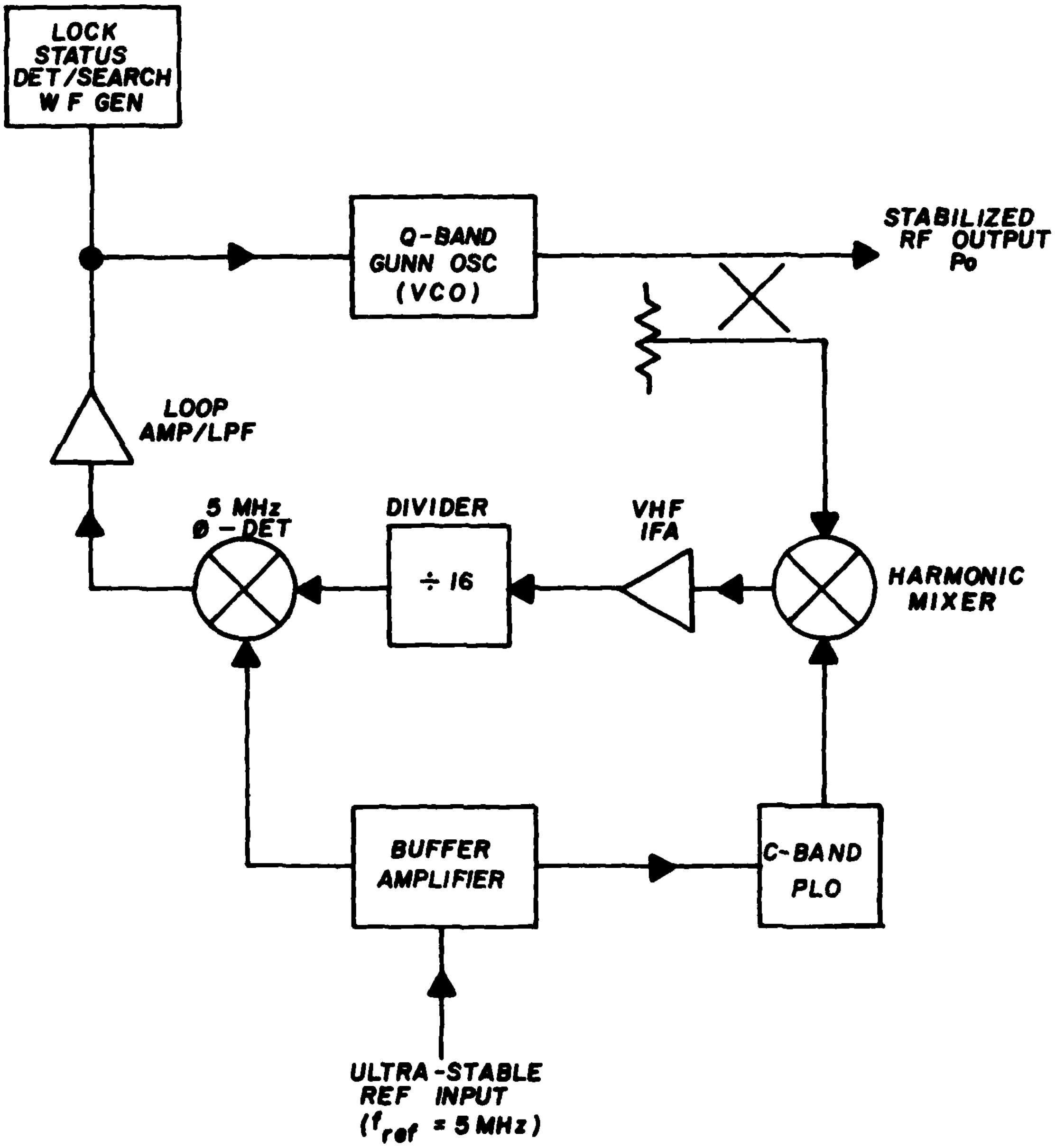
MEASURED POWER OUTPUT - FREQUENCY RESPONSE OF S/Q-BAND USUC



FUNCTIONAL BLOCK DIAGRAM OF THE Q-BAND PHASE LOCKED SOURCE

LNR COMMUNICATIONS INC

MEASURED POWER UPCONVERTER CHARACTERISTICS

	• Input frequency range	2-4 GHz
	• Pump frequency	41 GHz
	• Output frequency range	43-45 GHz
	• Upper sideband output power	95mW (avg.)
	• Passband output ripple	2 dB max. (P-P)
	• Lower sideband rejection	> 40 dB
	• S-band input power	100mW
	• Q-band pump power	400mW
	• S-band input VSWR	1.3:1 (max)
	• Q-band output VSWR	1.5:1 (max)
	• Q-band PLO output power	105mW
*	• Projected ILO output power	450mW

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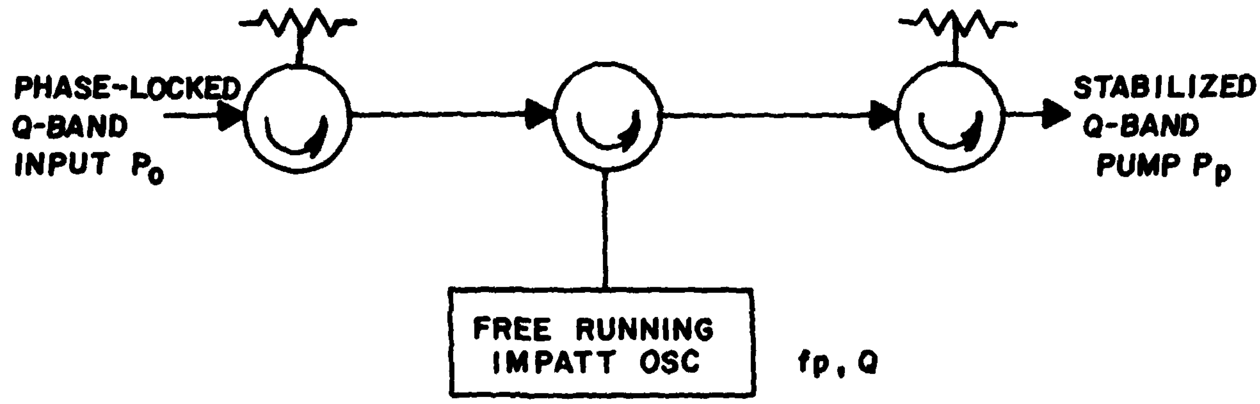
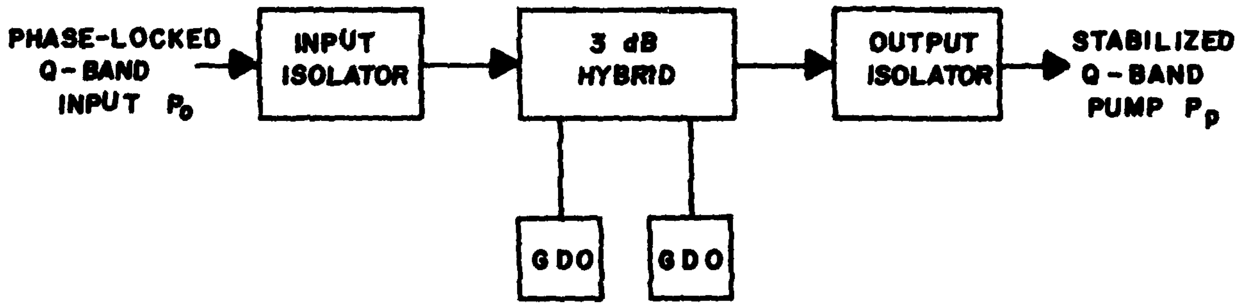


$$B_{LOCK} = \frac{2f_p}{Q} \sqrt{\frac{P_o}{P_p}} > \Delta f_{o\,p\text{-}p} \quad \text{(DRIFT)}$$

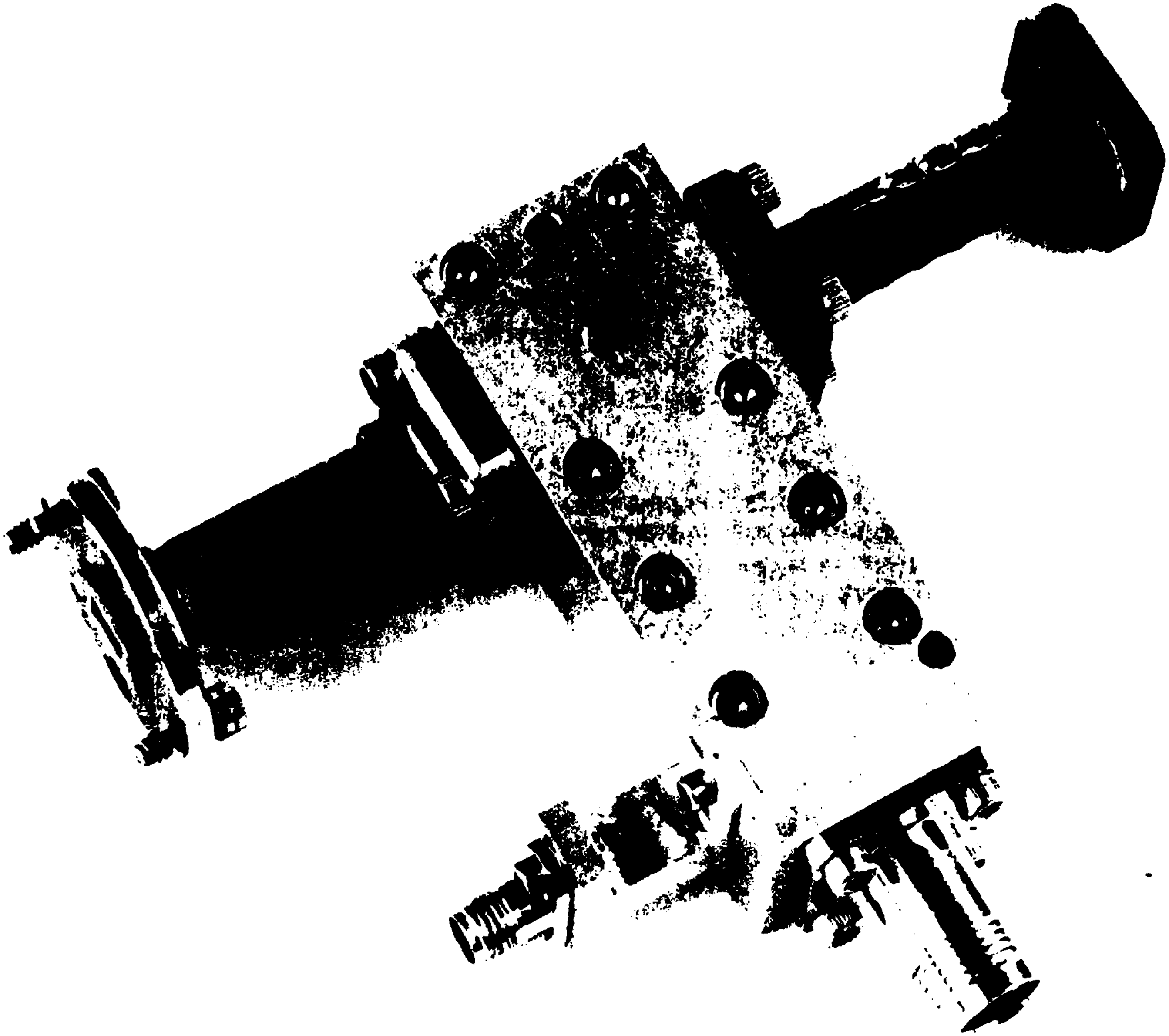
a) CIRCULATOR COUPLED IMPATT OSCILLATOR



b) HYBRID COUPLED GUNN DIODE OSCILLATORS

ALTERNATIVE INJECTION LOCKED OSCILLATOR CONFIGURATIONS

LNR COMMUNICATIONS INC



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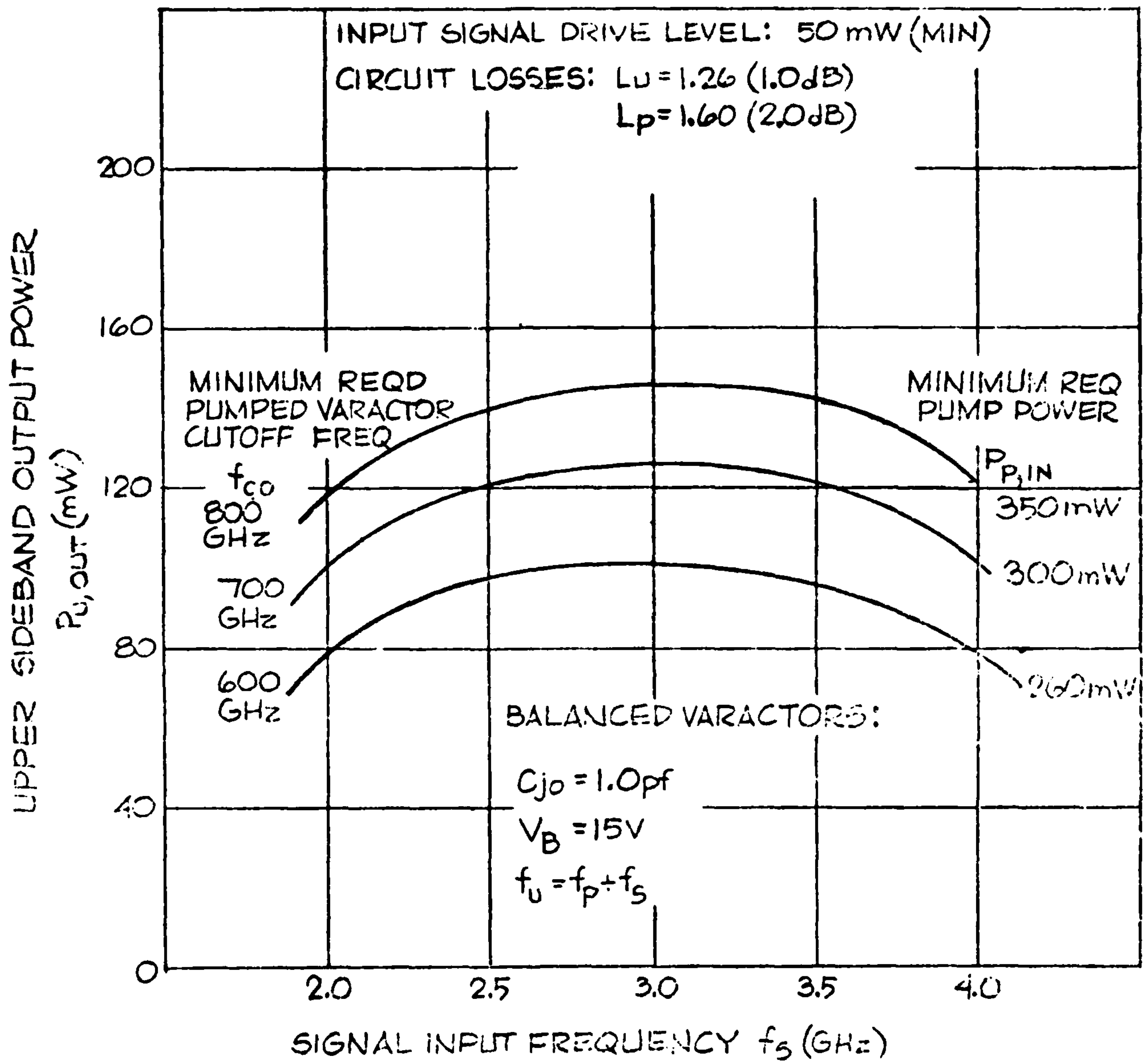
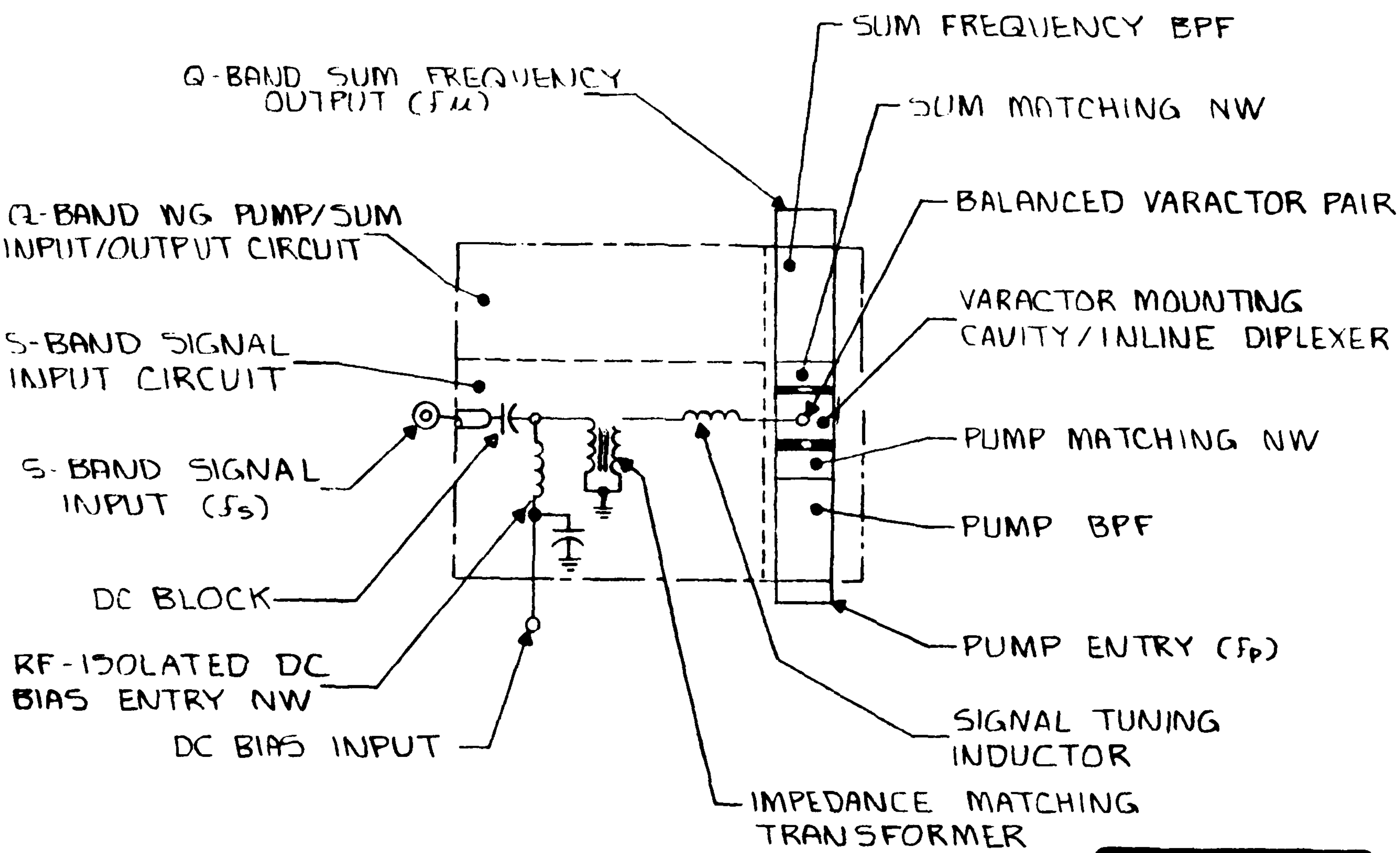
PHOTOGRAPH OF S/Q BAND USUC, INCLUDING IN-LINE PUMP/SUM DIPLEXER



THEORETICAL S-TO-Q-BAND HIGH POWER USUC OUTPUT POWER-FREQUENCY RESPONSE CURVES



SCHEMATIC LAYOUT OF S/Q-BAND USUC

PERFORMANCE GOALS OF HIGH POWER S/Q-BAND UPCONVERTER

• Input frequency range	2-4 GHz
• Pump frequency	41 GHz
• Output frequency range (USB)	43-45 GHz
• Upper sideband output power	100mW (Nom.)
• Passband output ripple	$\pm$1.5 dB (Max.)
• Lower sideband rejection	40 dB (Min.)
• S-band input power	100mW (Max.)
• Q-band pump	self-contained phase @ 41 GHz
• Q-band pump power	300mW (Nom.)
• Pump source phase locked loop (PLL) bandwidth	20 KHz (Nom.)
• Reference input frequency	5 MHz
• Pump source FM noise within PLL BW of carrier (fm 20 KHz)	$8.2 \times 10^3 \Delta f_{ref.}$ (rms Hz/$\sqrt{Mz}$)

HIGH POWER S/Q BAND SATCOM UPLINK TRANSMITTER UNCONVERTER

LNR Communications

H. C. Okean

HIGH POWER S/Q BAND SATCOM UPLINK TRANSMITTER UPCONVERTER

BY

H. DeGruyl, H.C. Okean and L.J. Steffek

Presented At

EHF SATCOM TECHNOLOGY WORKSHOP

San Diego, California
August, 1981

HIGH POWER S/Q BAND SATCOM UPLINK

TRANSMITTER UPCONVERTER*

by

H. deGruyl, H.C. Okean and L.J. Steffek
LNR Communications, Inc.

A 100mW output S-to-Q band varactor upper sideband up-converter (USUC), including associated phase locked solid state Q-band pump source, is being developed for use in the 44 GHz uplink transmitter sections of the 44/20 GHz Navy SATCOM ground terminals. Utilizing a balanced pair of in-house GaAs Schottky varactors embedded in a composite waveguide/TEM structure, said USUC translates a 2 GHz wide digitally modulated signal spectrum from the 2-4 GHz input to the 43-45 GHz upper sideband output bands. At 400 mW pump power at 41 GHz and 50 mW signal input level, the upper sideband output power ranges between 60 and 110 mW over 43-45 GHz, with better than 40 dB lower sideband rejection.

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*This effort was sponsored by the Naval Ocean Systems Center under Contract No. N00123-79-C-1529.

DEVELOPMENT STATUS FOR A 20 GHz FET SPACECRAFT TRANSMITTER

Texas Instruments

V. Sokolov

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TEXAS INSTRUMENTS
INCORPORATED

DEVELOPMENT STATUS FOR A 20 GHz FET SPACECRAFT TRANSMITTER*

BY

V. SOKOLOV, R.C. BENNETT, P. SAUNIER,
R.P. LINDSLEY, C.H. MOORE, AND R.E. LEHMANN

TEXAS INSTRUMENTS INCORPORATED
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P.O. BOX 225936
MAIL STATION 134
DALLAS, TEXAS 75265

*THIS WORK IS SUPPORTED BY NASA (LERC) UNDER CONTRACT NO. NAS3-22504

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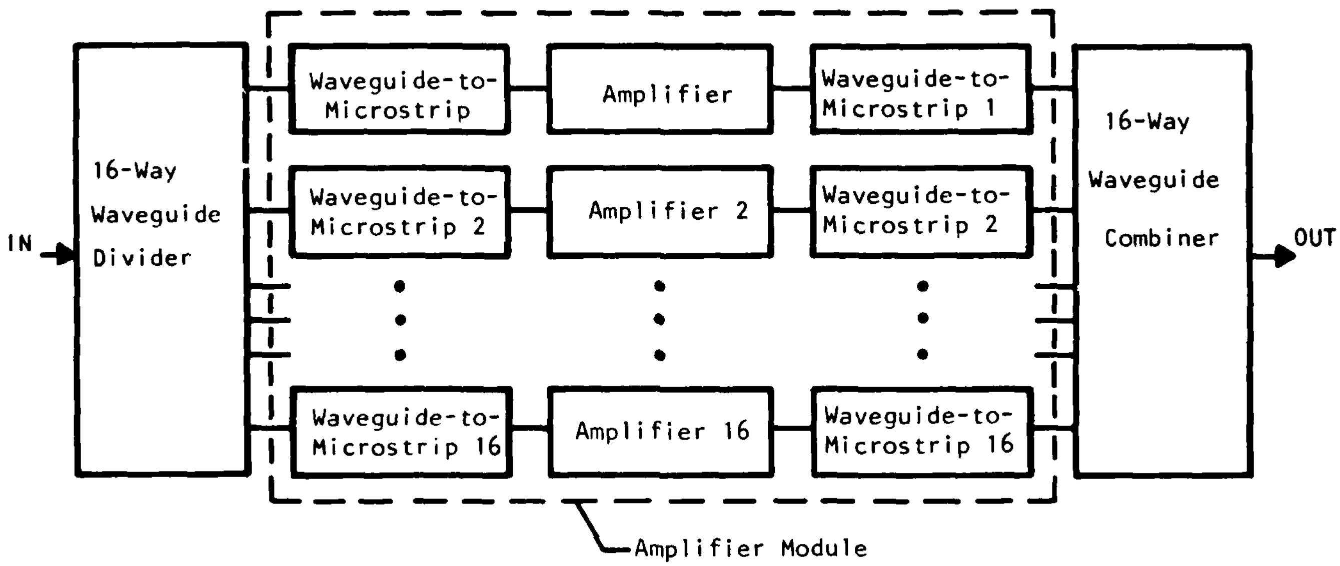
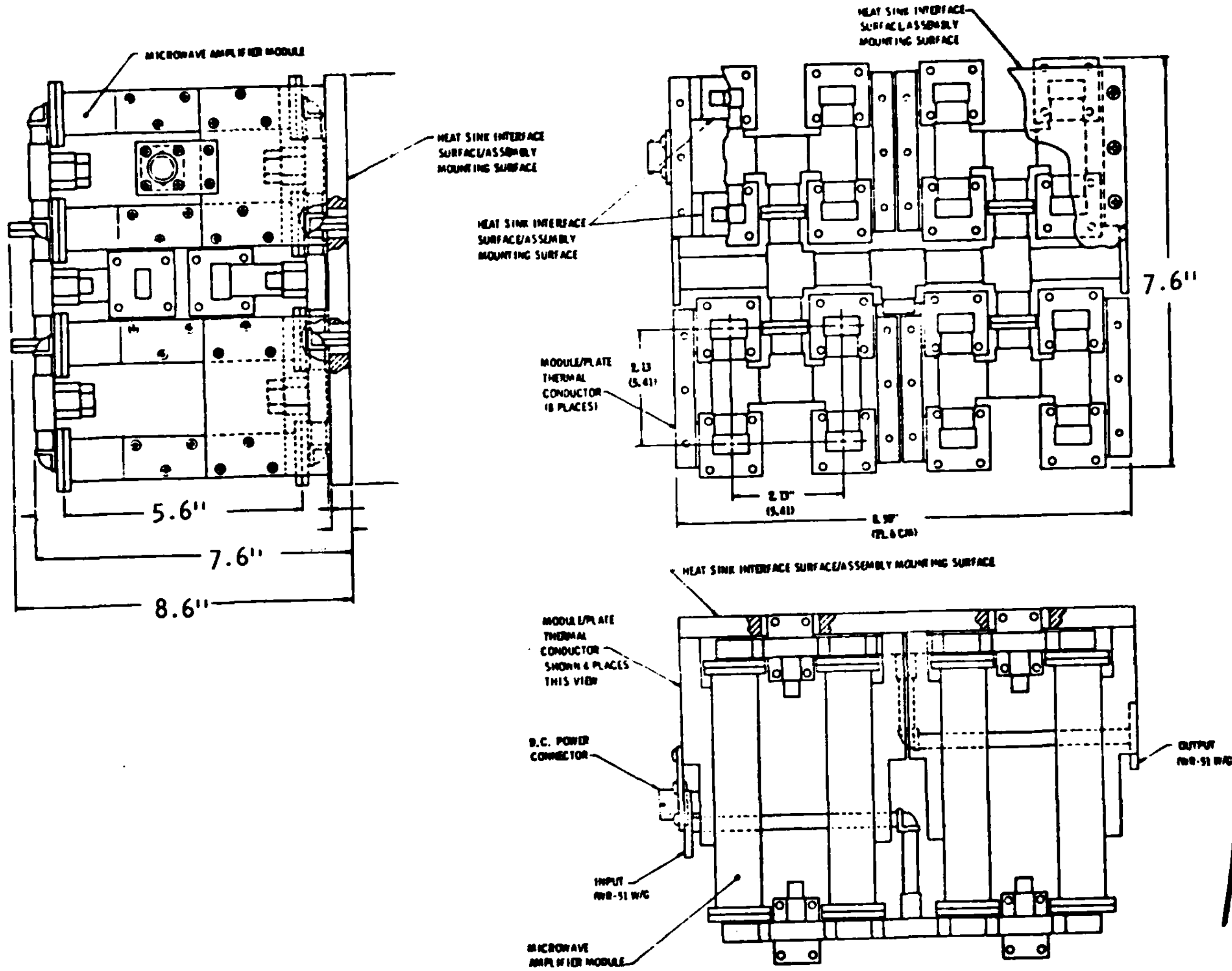
BASIC PERFORMANCE SPECIFICATIONS
(GOALS)
INTEGRATED POC MODEL POWER AMPLIFIER

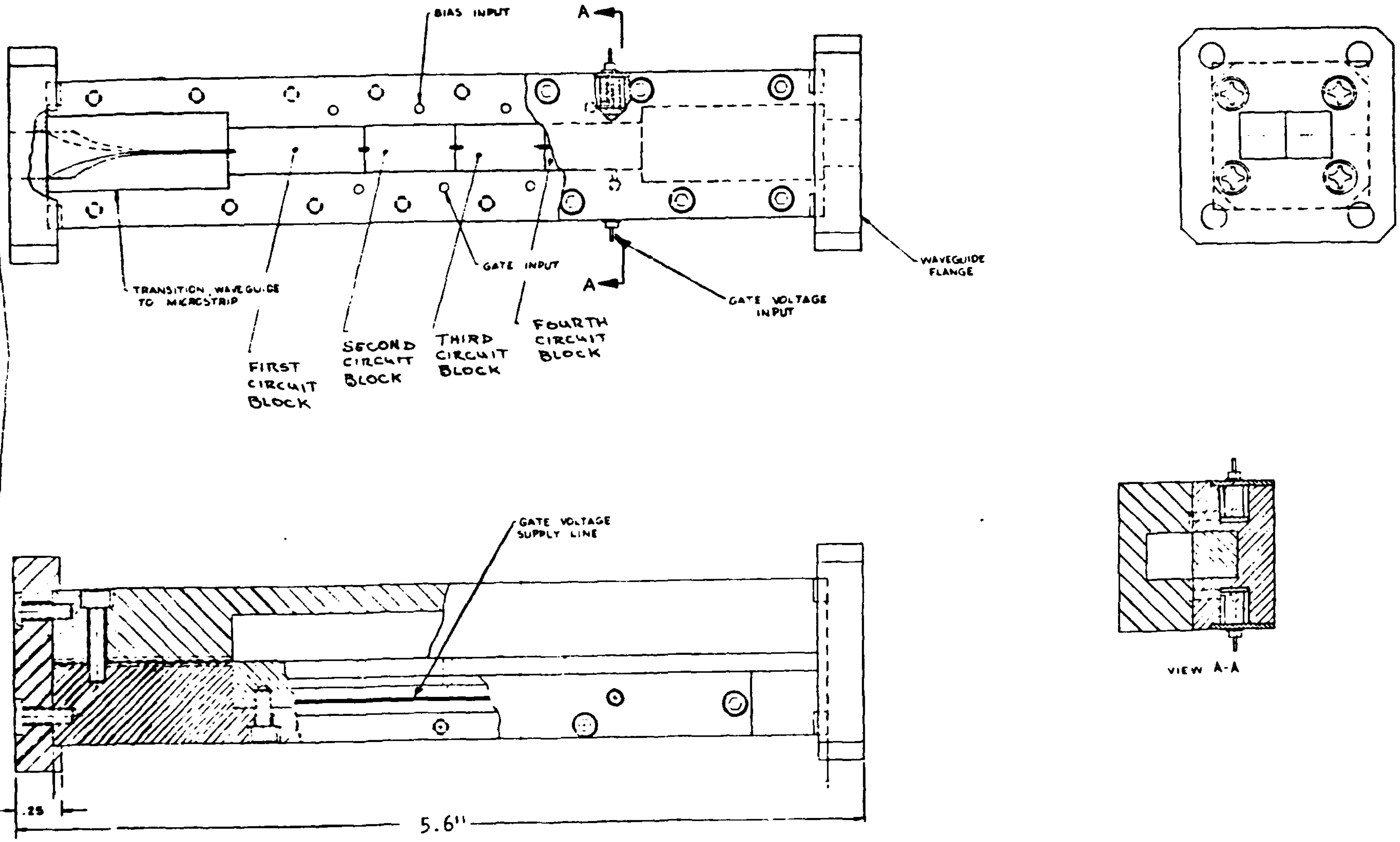
- Center Frequency: 19 GHz (F_0)
- RF Gain at F_0: 30 dB
- Output Power at F_0: 7.5 W (P_0)
- 1 dB Bandwidth: 17.7-20.2 GHz
- Efficiency at P_0: 10%
- Third Order Intermodulation Products: At least 20 dBc at P_0
- RF Connectors: WR-51 Waveguide
- Operation of POC Model Over 0°-75°C Baseplate Temperature Range



Block Diagram of General Design Approach



20 GHz Amplifier Assembly Single Surface for Mounting and Heat Transfer



Amplifier Module Assembly

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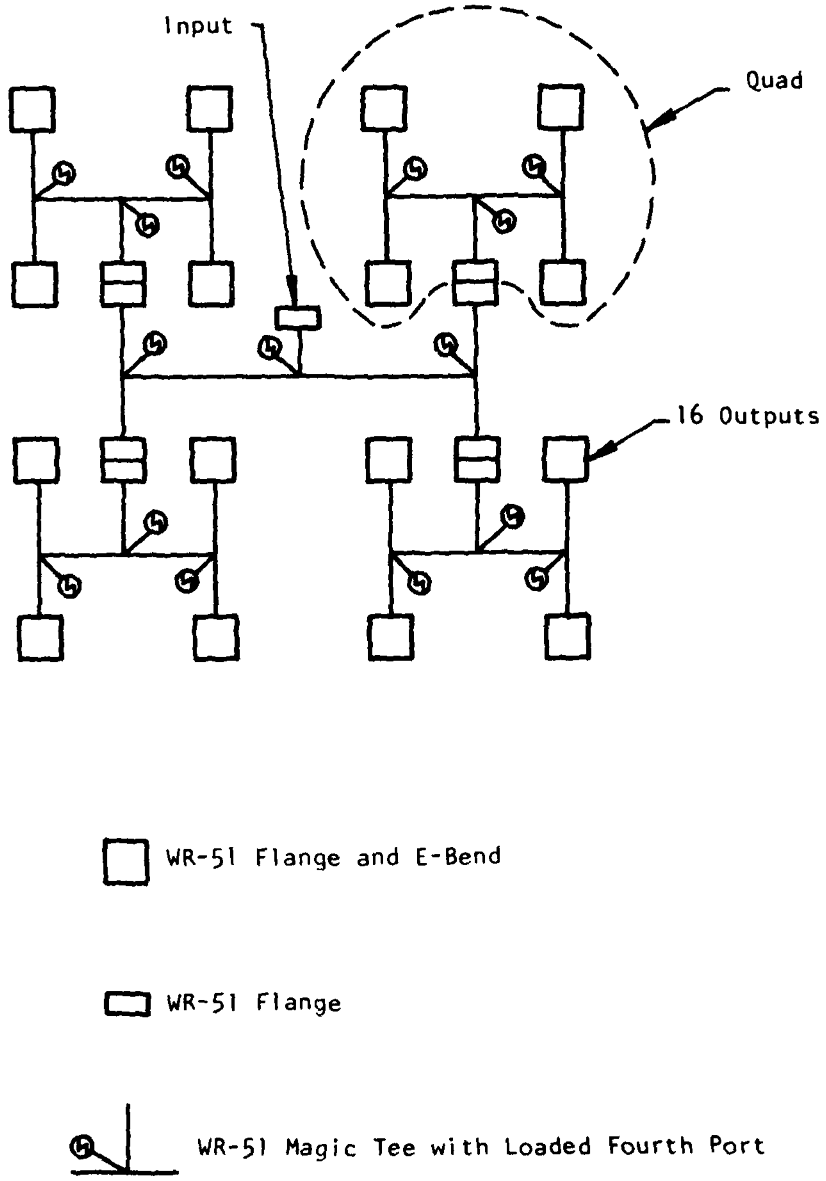
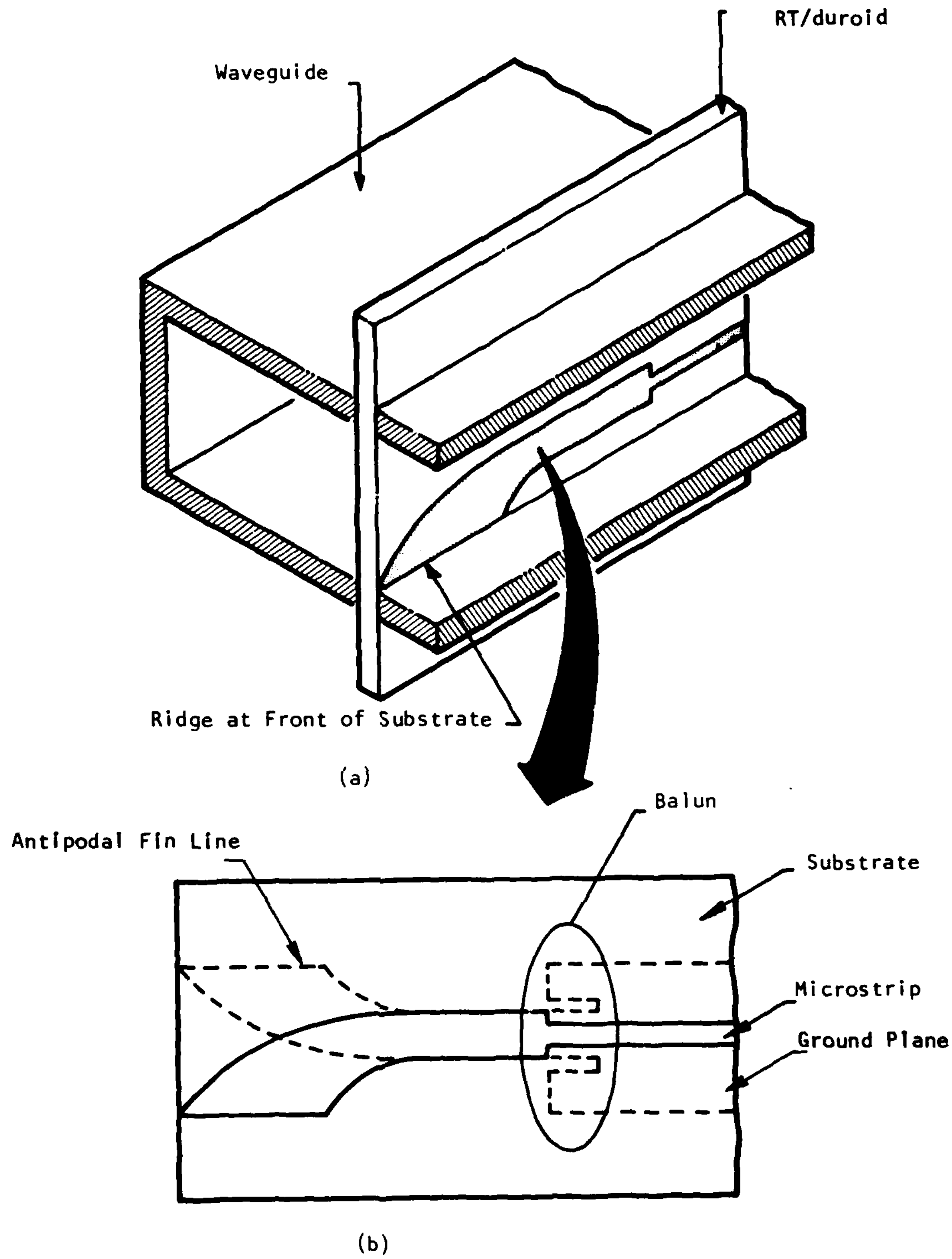
DEVELOPMENT STATUS FOR A 20 GHz
FET SPACECRAFT TRANSMITTER

OUTLINE

- AMPLIFIER PERFORMANCE GOALS
- AMPLIFIER BLOCK DIAGRAM
- 20 GHz FET DEVICES
- WAVEGUIDE DIVIDER/COMBINER DEVELOPMENT AND AMPLIFIER ASSEMBLY DRAWINGS
- AMPLIFIER MODULE DEVELOPMENT
- STATUS AND SUMMARY

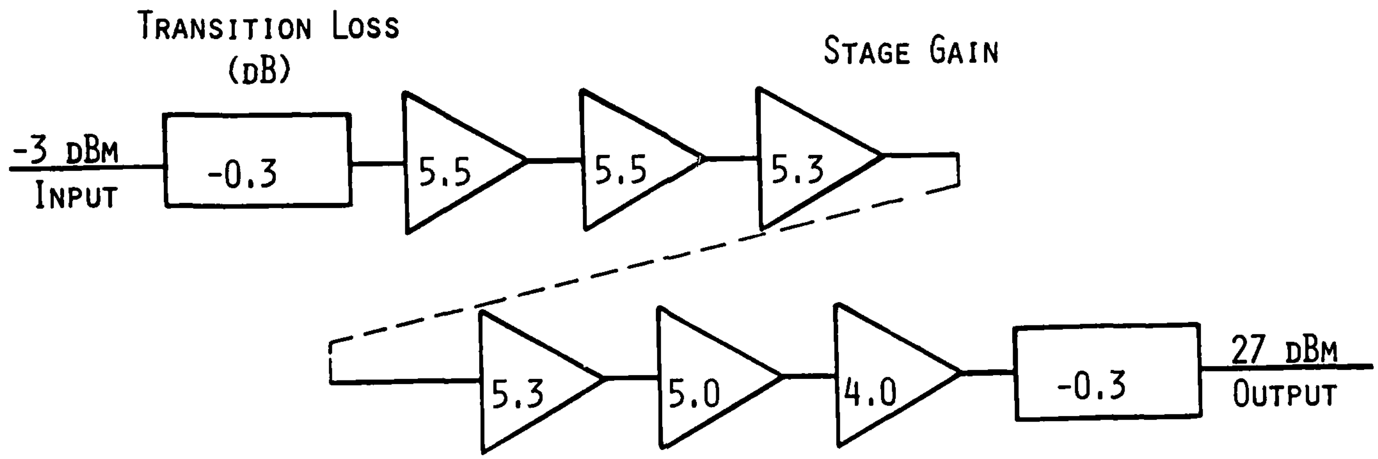


Block Diagram of Power Divider/Combiner



A Low-Loss Transition from Waveguide to Microstrip
(a) Outline of the substrate
inserted in the waveguide. (b) Position of the
planar circuit in the waveguide.

MODULE AMPLIFIER BLOCK DIAGRAM
(BREADBOARD VERSION)



150	150	150	FET GATE WIDTH (MICRONS)
300	1350	2x1350	
30	30	30	NOMINAL DRAIN CURRENT (mA)
60	250	500	

NOMINAL DRAIN VOLTAGE ~7 V

GaAs FET DESIGN AND FABRICATION

- Device Type
- Performances
- Status of Device Supply

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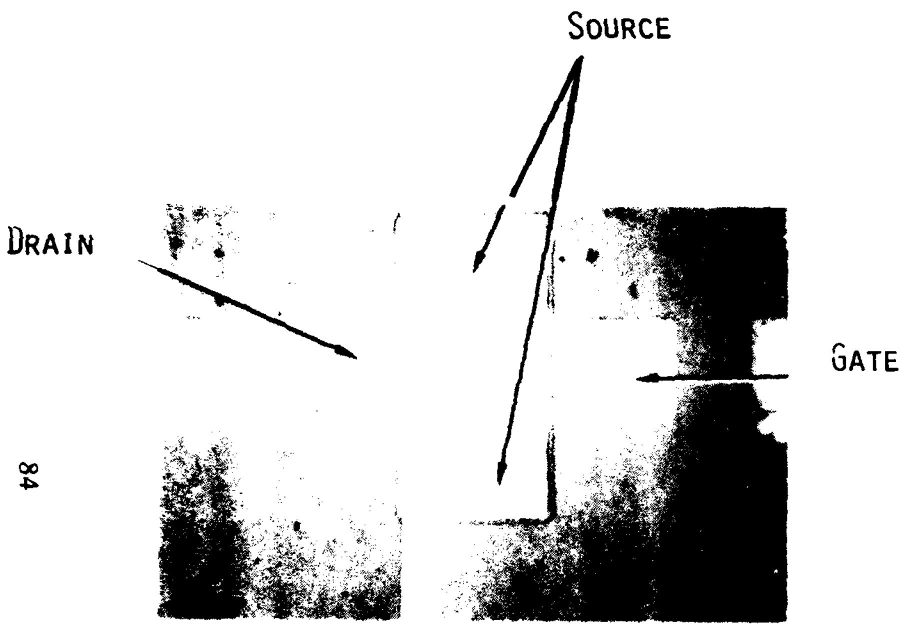
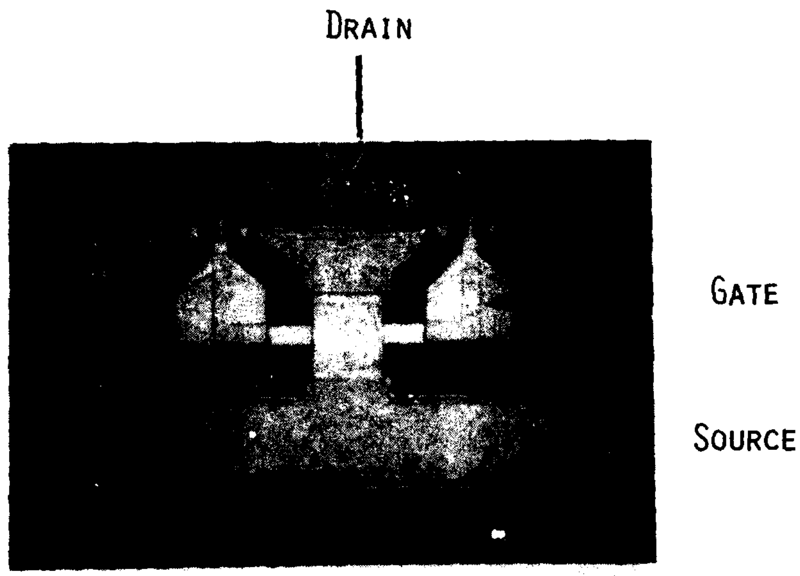


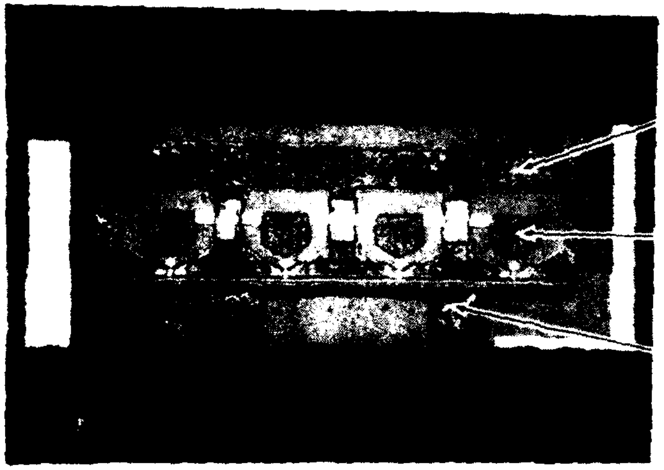
150 μm Gate Width Device



300 μm Gate Width Device

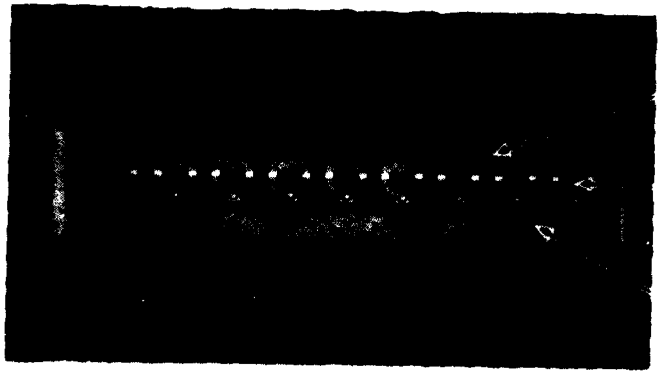
20 GHz FETs

Texas Instruments Incorporated



600 µm Gate Width FET

Chip Dim: 0.76 x 0.3 mm



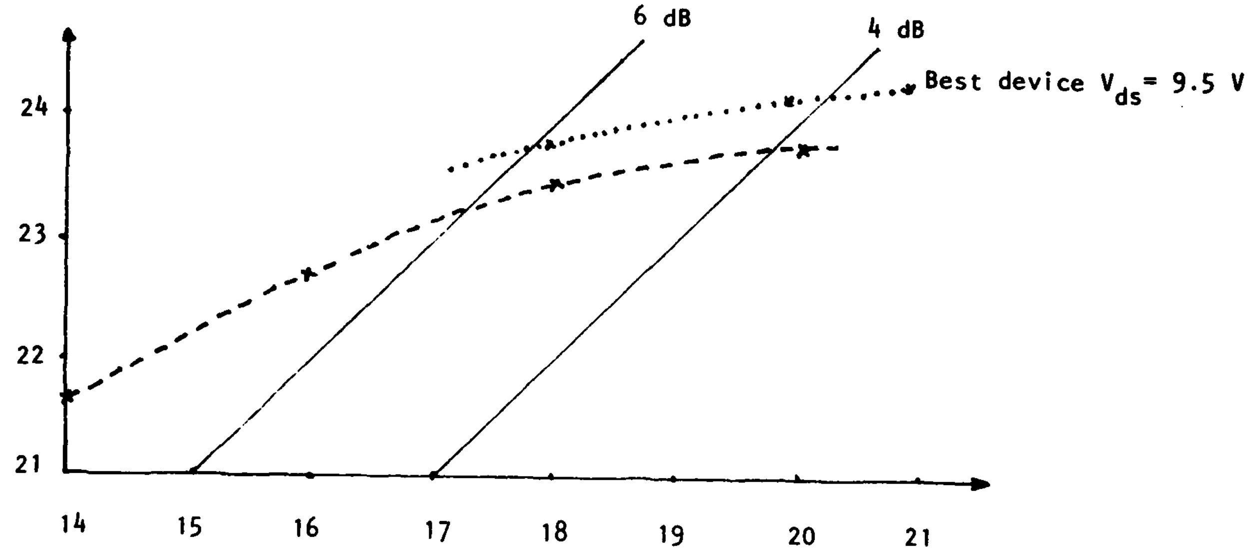
1350 µm Gate Width FET

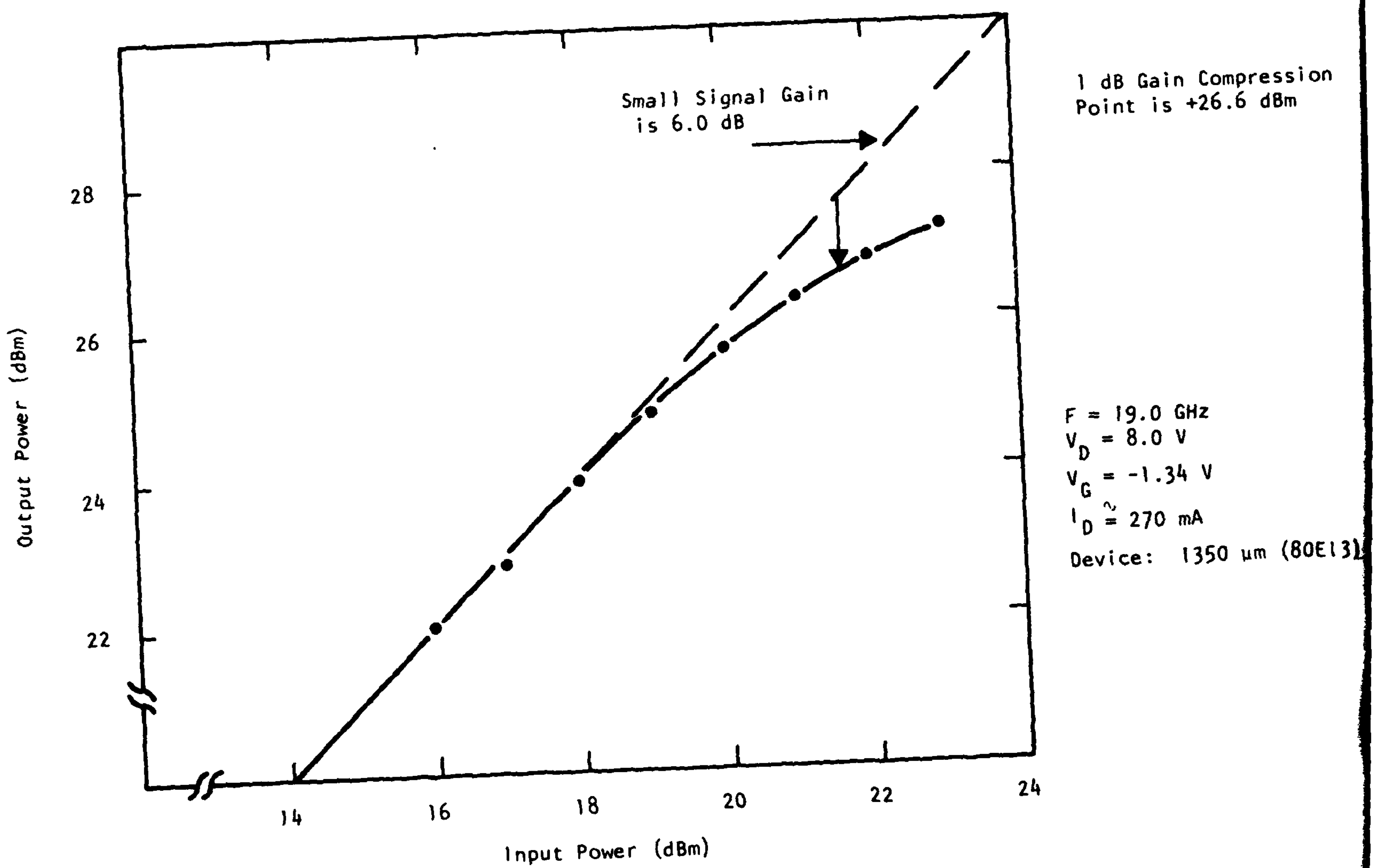
Chip Dim: 1.5 x 0.3 mm

20 GHz FETs

PERFORMANCES

- Tests are performed on 300 μm gatewidth devices at 15 GHz
- Small signal gain with 5 V on the drain (5 dBm input power) 9 to 10.5 dB
- Input power versus output power with 8 V on the drain





Gain Compression Curve for 1350 μm π-Gate FET
(In 5th Stage Amplifier Circuit)

DEVICES

<u>STATUS</u>

- ABOUT 150 π GATE 1350 μM DEVICES ARE AVAILABLE
- A SUFFICIENT NUMBER OF 150 μM AND 300 μM DEVICES HAVE BEEN FABRICATED FOR IMMEDIATE NEED

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16-WAY MANIFOLD REQUIREMENTS

PURPOSE: THE POWER DIVIDER/COMBINER WILL PROVIDE UNIFORM AMPLITUDE AND PHASE TO EACH OF 16 AMPLIFIER MODULES, AND WILL RECOMBINE THE OUTPUT POWER OF THE 16 MODULES FOR MAXIMUM EFFICIENCY

ELECTRICAL

PARAMETER	DESIGN GOAL
FREQUENCY	17.7 TO 20.2 GHZ
VSWR, INPUT	1.25:1 MAX
AMPLITUDE VARIATION	± 0.2 DB
PHASE VARIATION	± 5.0 DEGREES
INSERTION LOSS	0.8 DB MAX
ISOLATION (BETWEEN OUTPUTS)	20 DB MIN

MECHANICAL

WEIGHT	1.6 POUNDS MAX
SIZE	COMPATIBLE WITH OVERALL PACKAGING CONCEPT
INPUT PORT	1, WR-51 WAVEGUIDE
OUTPUT PORT	16, MODULE COMPATIBLE WR-51

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20 GHZ MANIFOLD DESIGN

- A SINGLE MANIFOLD CONSISTS OF A 16-WAY MATCHED WAVEGUIDE POWER DIVIDER.
- LIGHT WEIGHT, DIP-BRAZED ALUMINUM CONSTRUCTION OFFERS LOW LOSS PERFORMANCE.
- FOUR "QUADS" PER MANIFOLD ASSEMBLY OFFERS MODULAR CONSTRUCTION.
- THE MODULAR HEAT SINK DESIGN PROVIDES EASY INTERFACE WITH A COLD PLATE.
- A PAIR OF MANIFOLDS FOR EACH PROOF-OF-CONCEPT TRANSMITTER ALLOWS POWER DIVISION AT THE INPUT AND LOW LOSS POWER COMBINING AT THE OUTPUT.
- STANDARD TEST EQUIPMENT FLANGES (HEWLETT PACKARD STYLE) ARE PROVIDED ON THE INPUT/OUTPUT PORTS.

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MECHANICAL DATA

RF INPUT INTERFACE	WR-51 WAVEGUIDE FLANGE (HEWLETT PACKARD VERSION)
RF OUTPUT INTERFACE	WR-51 WAVEGUIDE FLANGE (HEWLETT PACKARD VERSION)
D.C. POWER INPUT	MS TYPE CONNECTOR MS3101R-20-16P
MOUNTING	INTERFACE SURFACE ACTS AS MOUNTING SURFACE AS WELL AS THERMAL CONDUCTOR
WEIGHT	13.8 LBS.
SIZE (CLEARANCE)	8.60 IN. X 8.50 IN. X 7.60 IN.
VOLUME (MAX)	556 $IN.^3$

THERMAL DESIGN

REQUIREMENTS (WORST CASE)

A. MAXIMUM DEVICE TEMPERATURE - 100°C
B. MAXIMUM TEMPERATURE VARIATION BETWEEN MODULES - 10°C
C. OPERATE IN A 75°C ENVIRONMENT

ANALYSIS DATA

AMPLIFIER CARRIER TEMPERATURE

FIRST AMPLIFIER ASSEMBLY	(.72W)	90°C
SECOND AMPLIFIER ASSEMBLY	(.48W)	90°C
THIRD AMPLIFIER ASSEMBLY	(2.0W)	94°C
FOURTH AMPLIFIER ASSEMBLY	(4.0W)	99°C

HEAT SINK/MOUNTING PLATE 75°C

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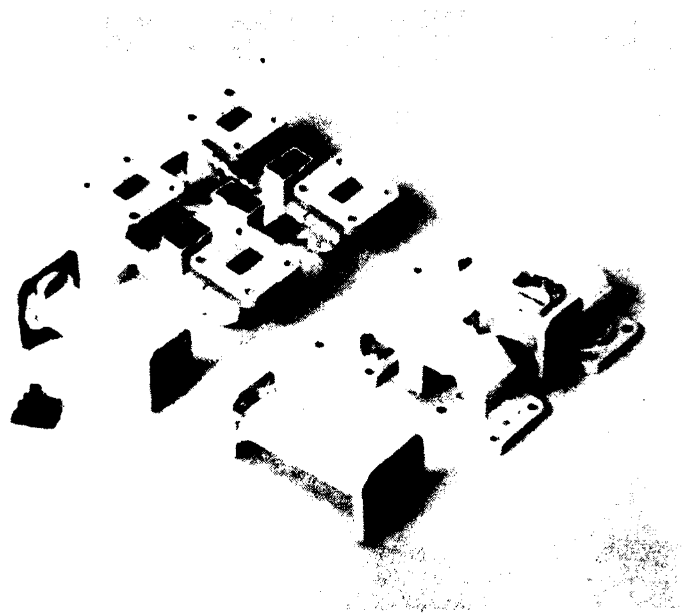
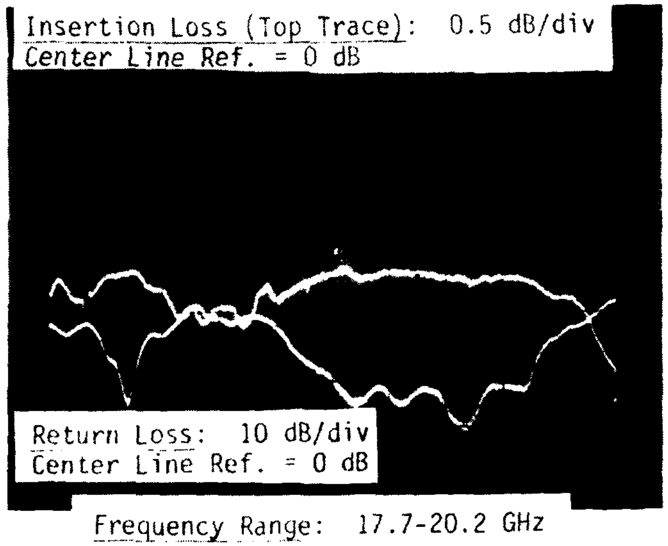
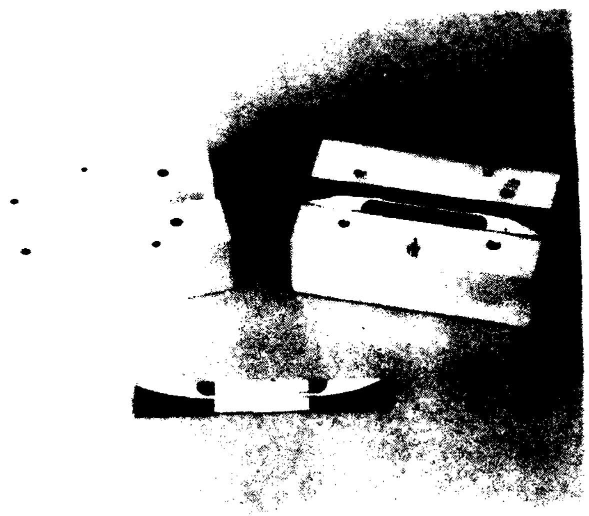


TWO QUAD ASSEMBLIES TERMINATION BLOCK, AND FLANGE ADAPTURS



RF PERFORMANCE OF A PAIR OF BACK TO BACK QUAD ASSEMBLIES (FIRST ASSEMBLY, PRELIMINARY RESULTS ONLY)



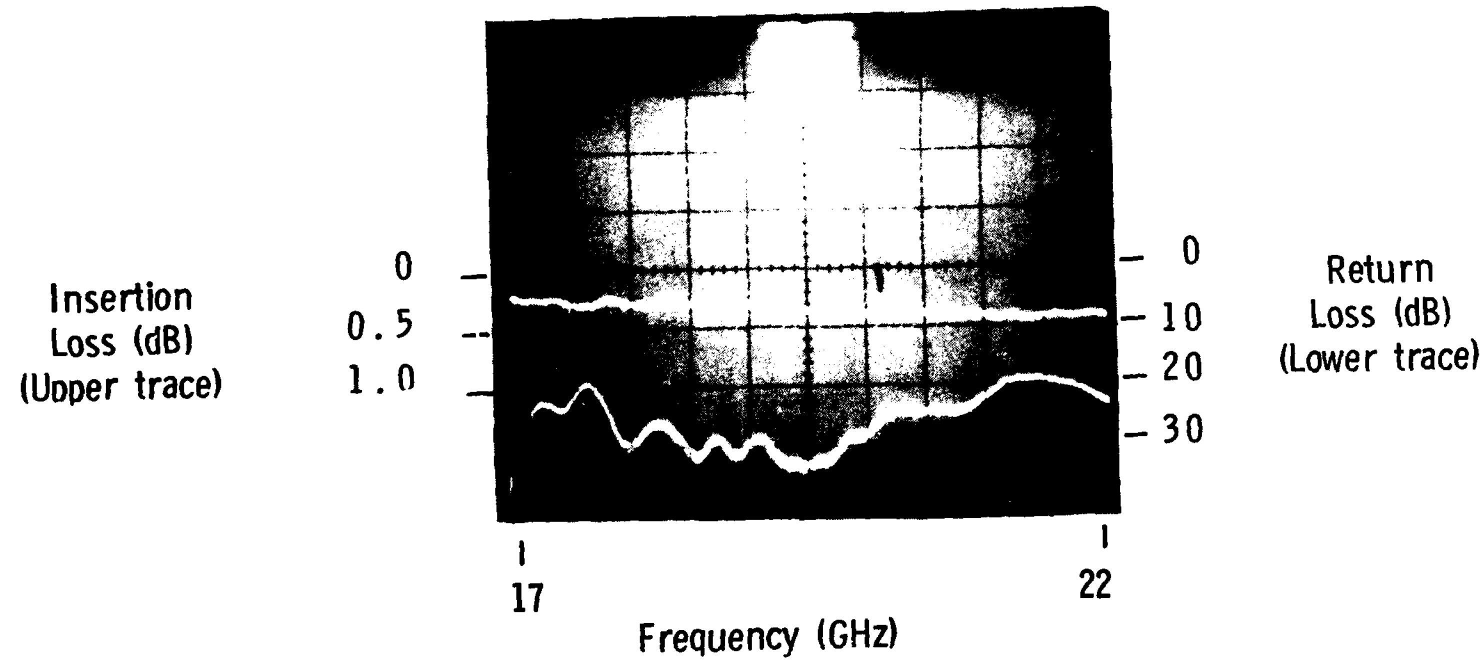
Waveguide-to-Microstrip Transition
Test Fixture and Test Circuit

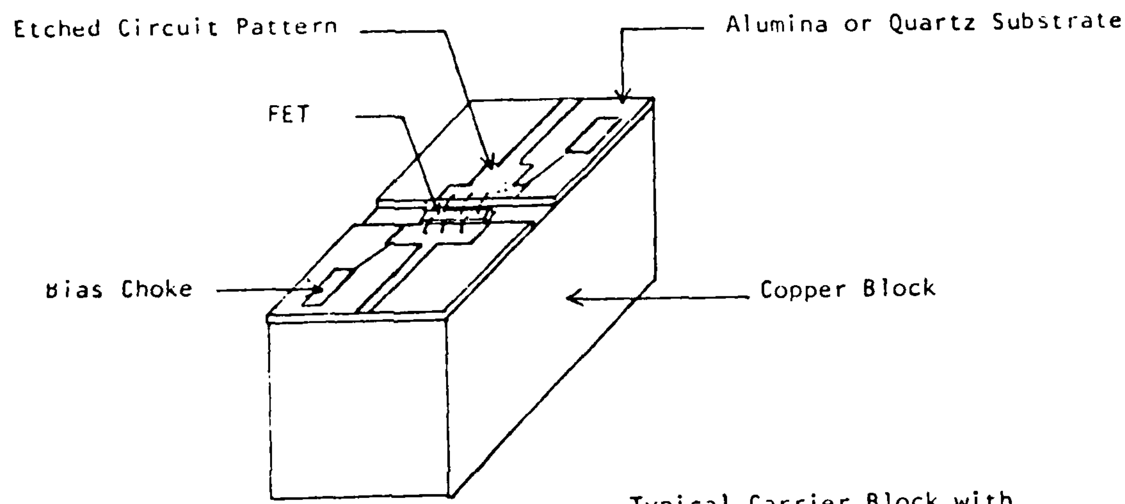
FREQUENCY RESPONSE

OF

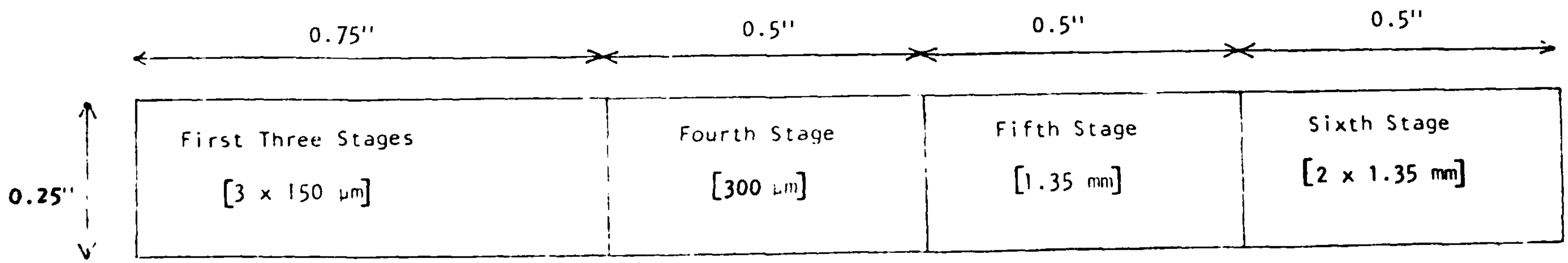
TWO WAVEGUIDE-TO-MICROSTRIP TRANSITIONS

(BACK-TO-BACK)





Typical Carrier Block with Microstrip Impedance Matching Circuit



Length of Four Blocks - 2.25''

Transition Length - ~ 1.50'' each

Total Module Length - ~ 5.25''

FET Carrier Blocks Used in Breadboard Amplifier